

FIG.1

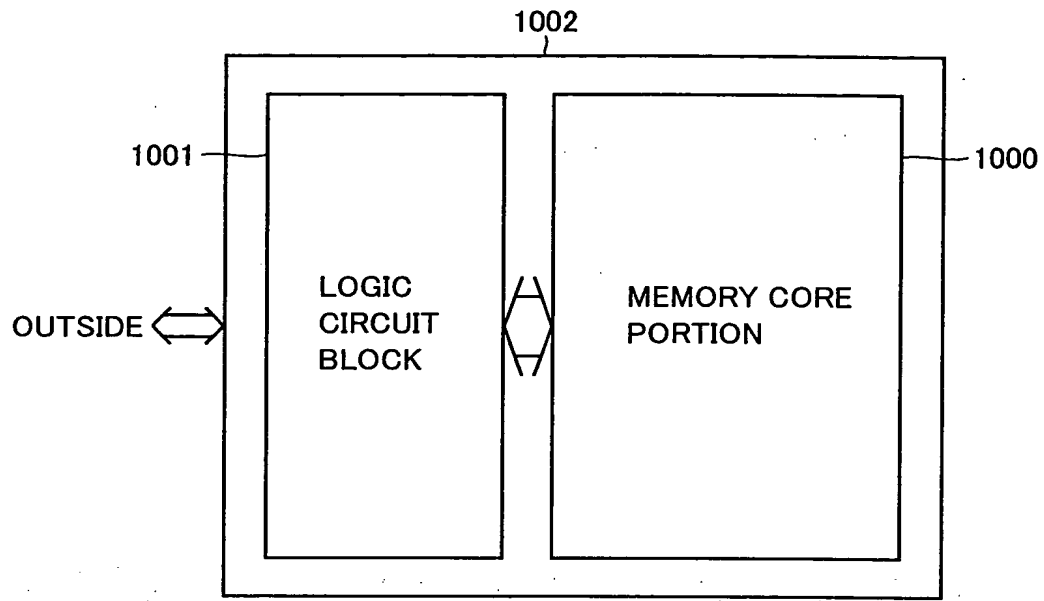


FIG.2

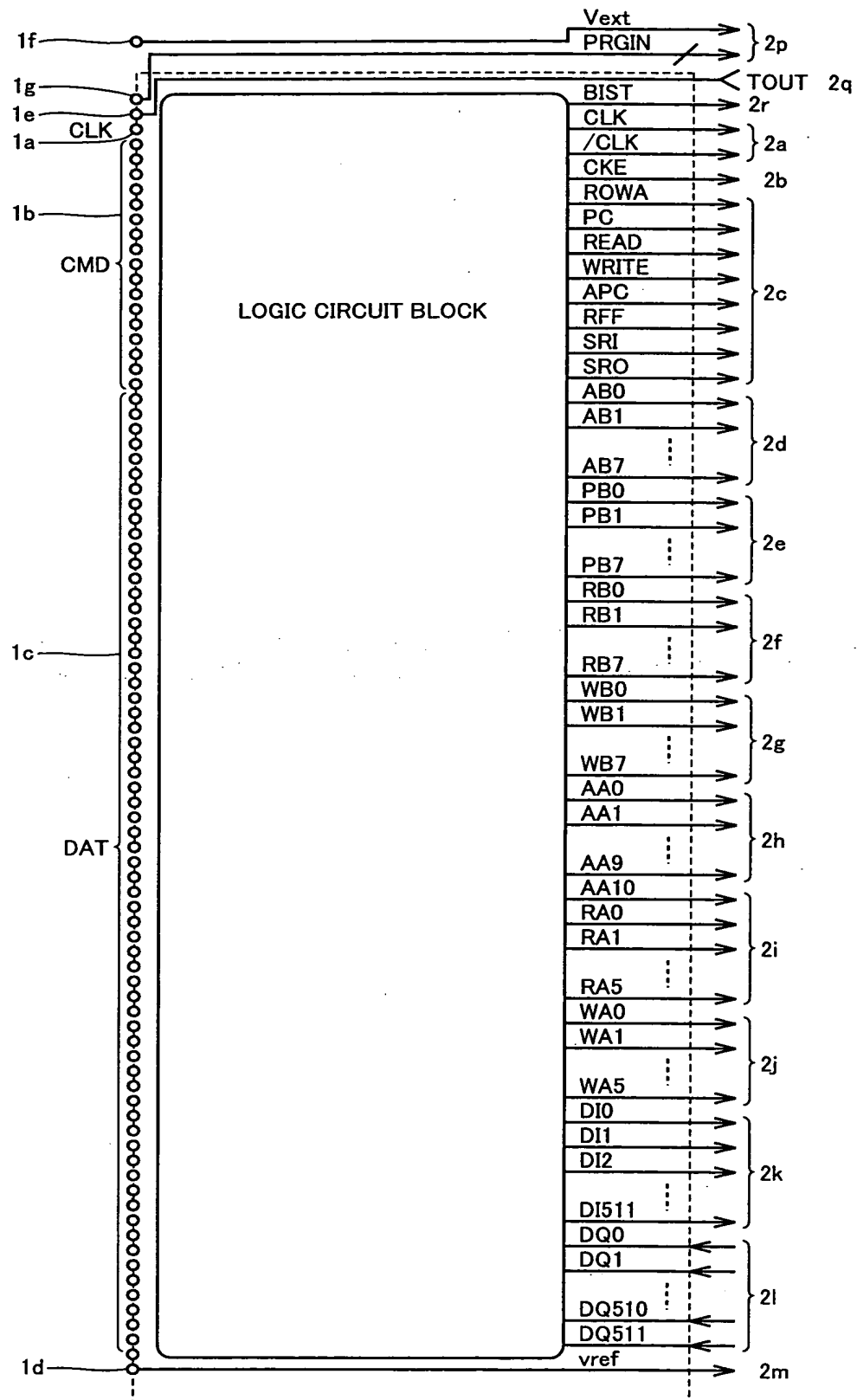


FIG.3

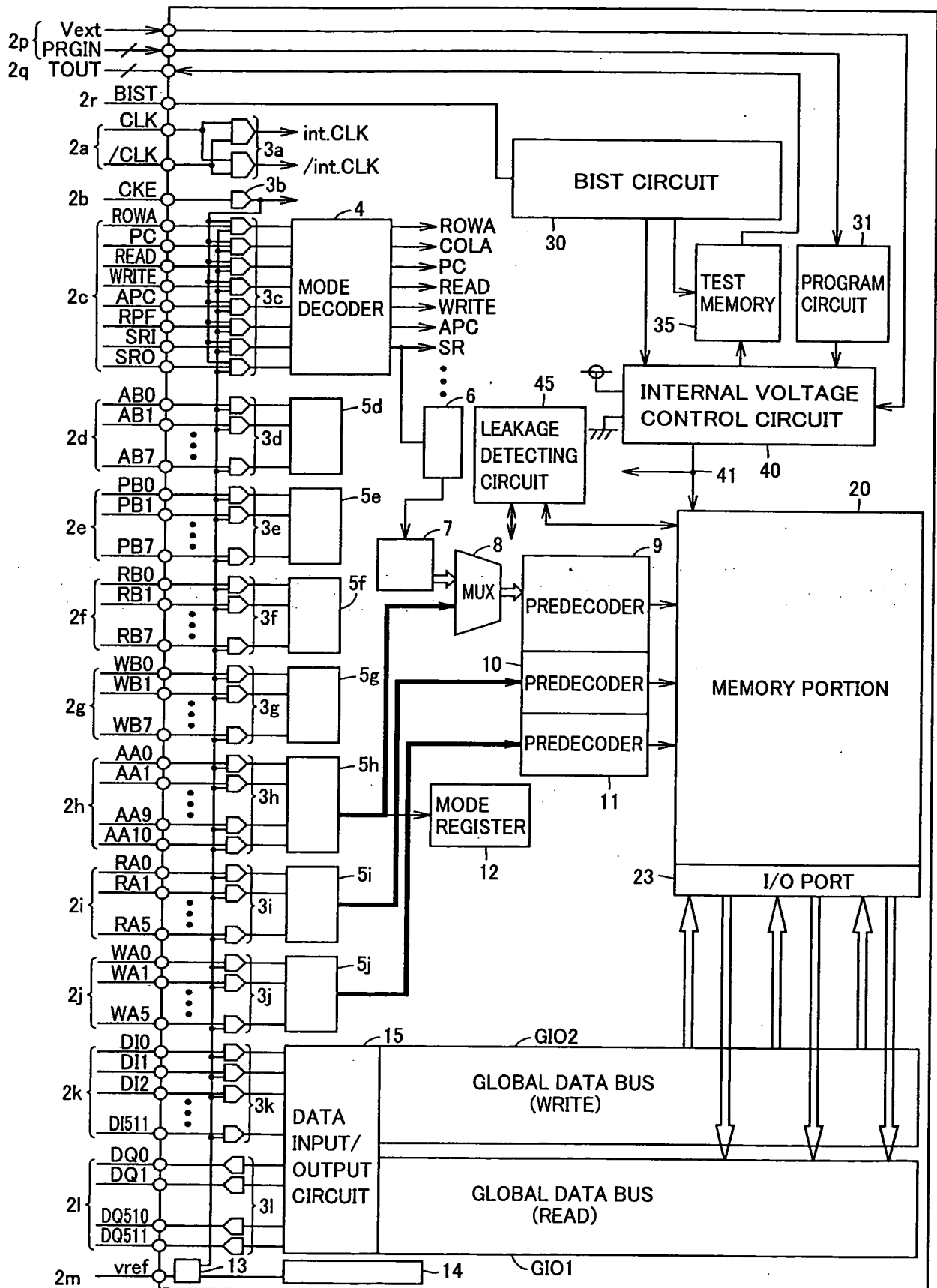


FIG.4

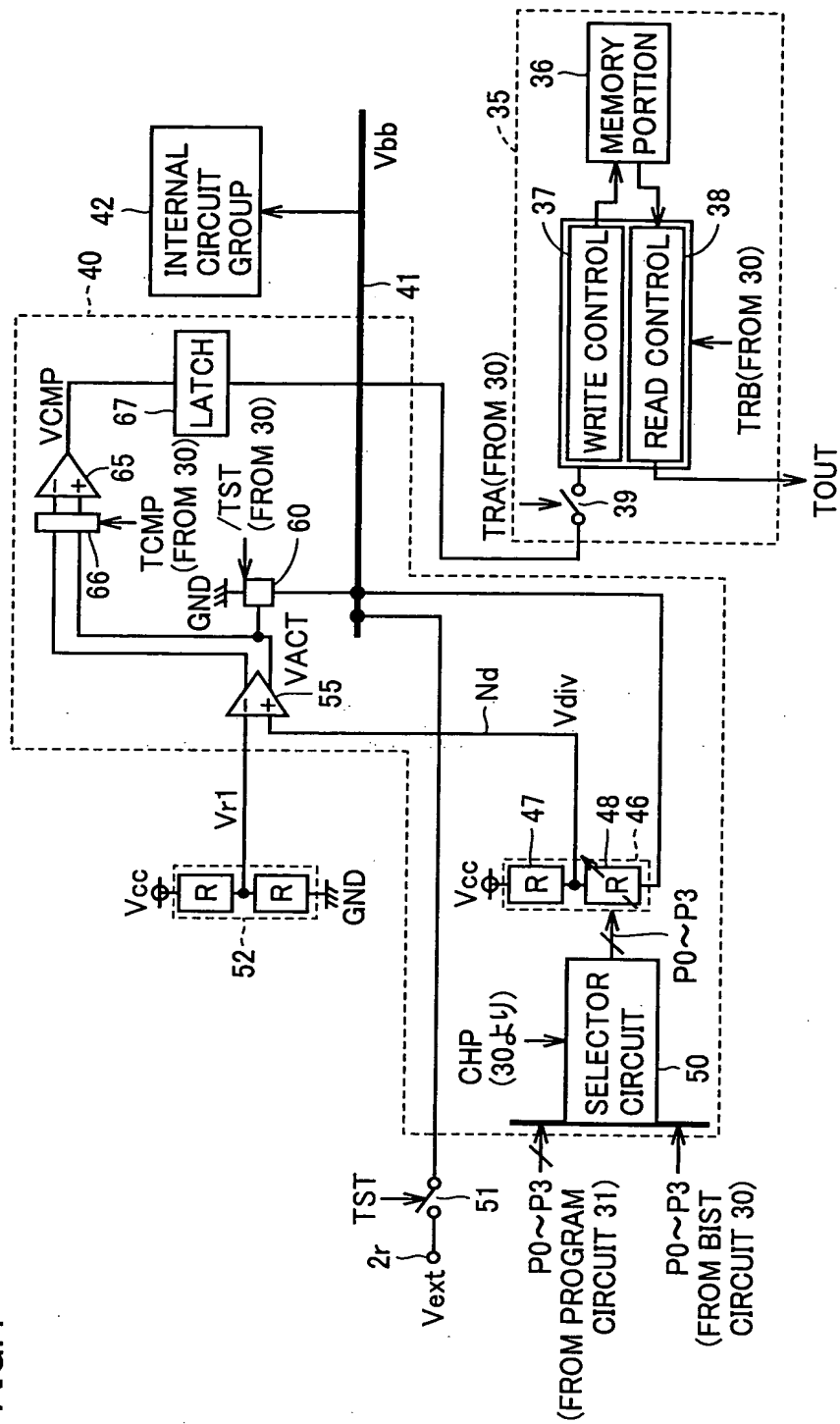


FIG.5

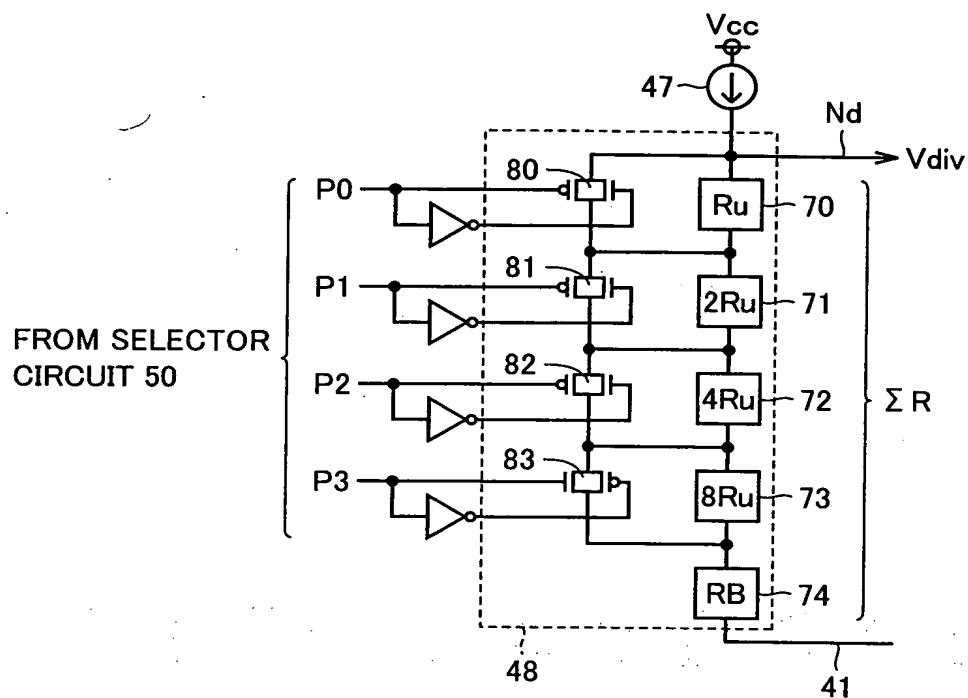


FIG.6

		LOW V _{bb} ← → HIGH V _{bb}															
ADJUSTMENT LEVEL		-8	-7	-6	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5	+6	+7
ADJUSTMENT SIGNALS (FROM BIST CIRCUIT 30)	P0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	P1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	P2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	P3	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
VCMP LEVEL		H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L
OUTPUT OF EX-OR 93		L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L

↓
 ADJUSTMENT
 SIGNALS
 ACCUMULATED
 TO MEMORY 36

P0=1
 P1=0
 P2=1
 P3=1

FIG.7

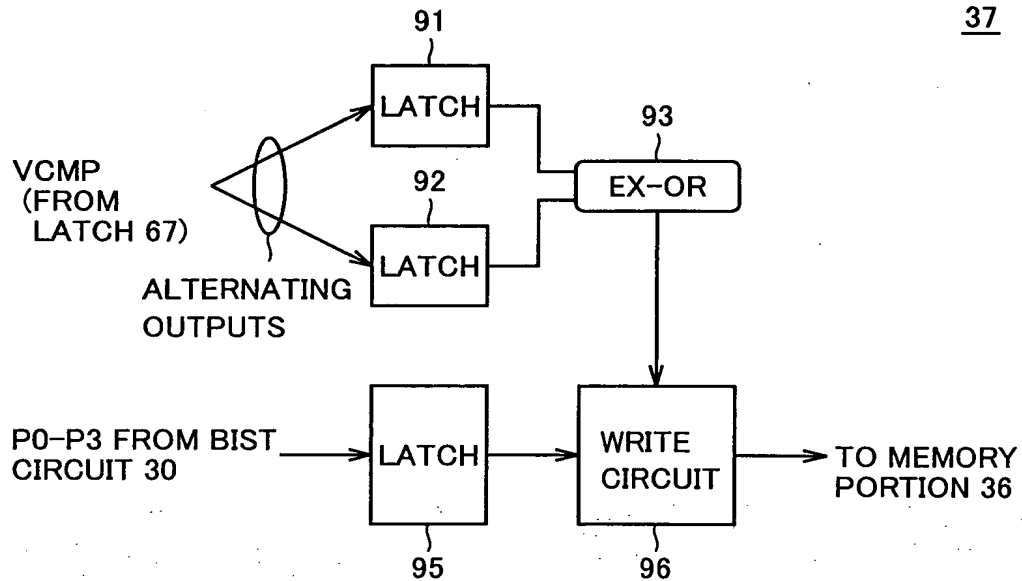


FIG. 8

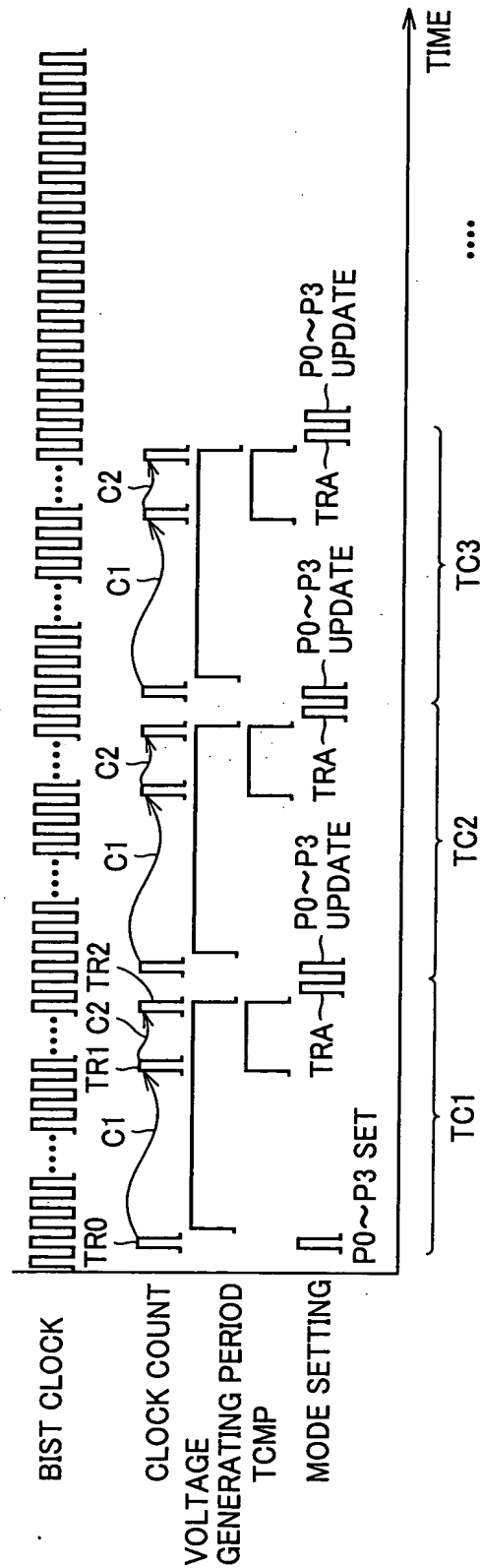


FIG. 9

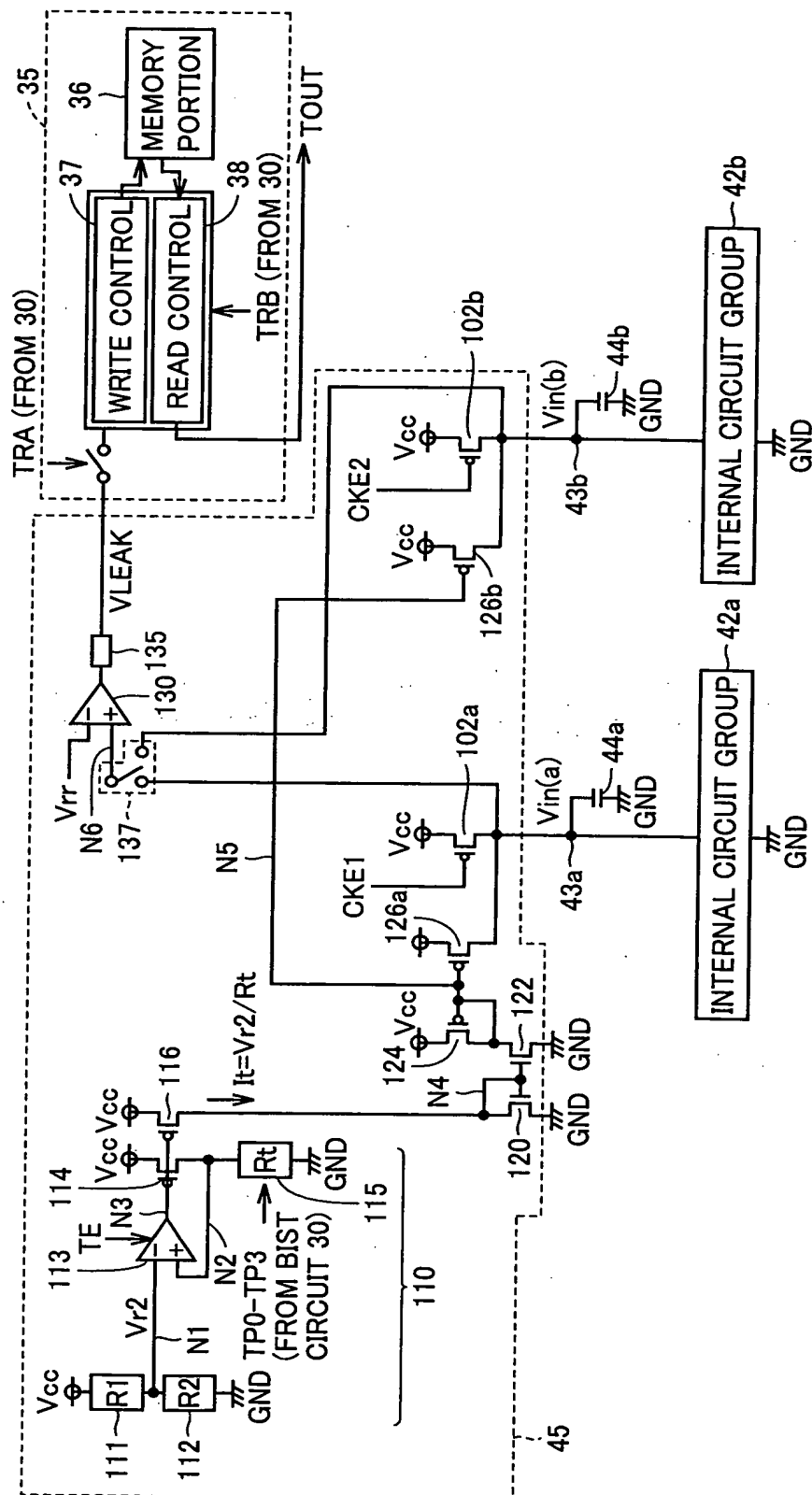


FIG.10

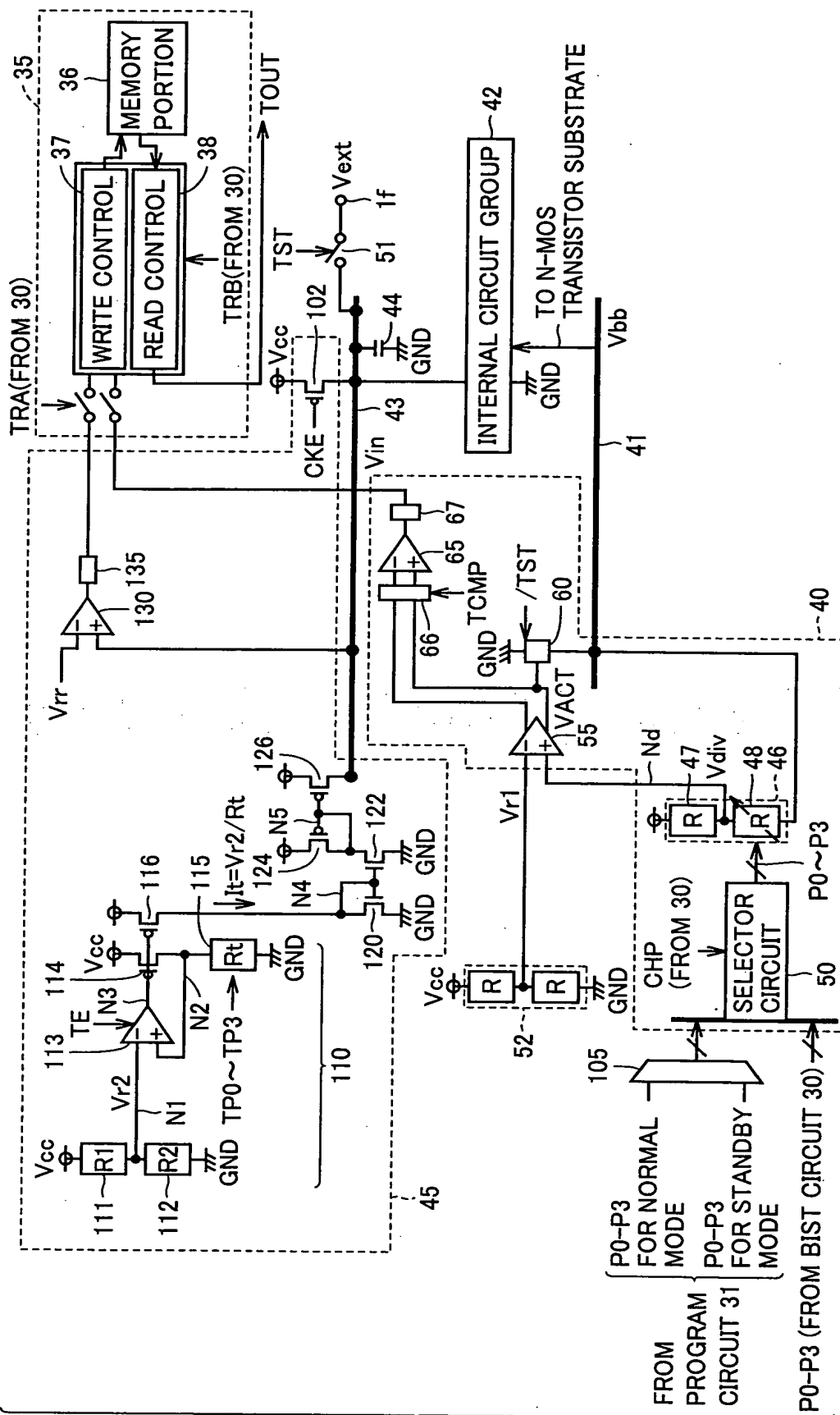


FIG.11

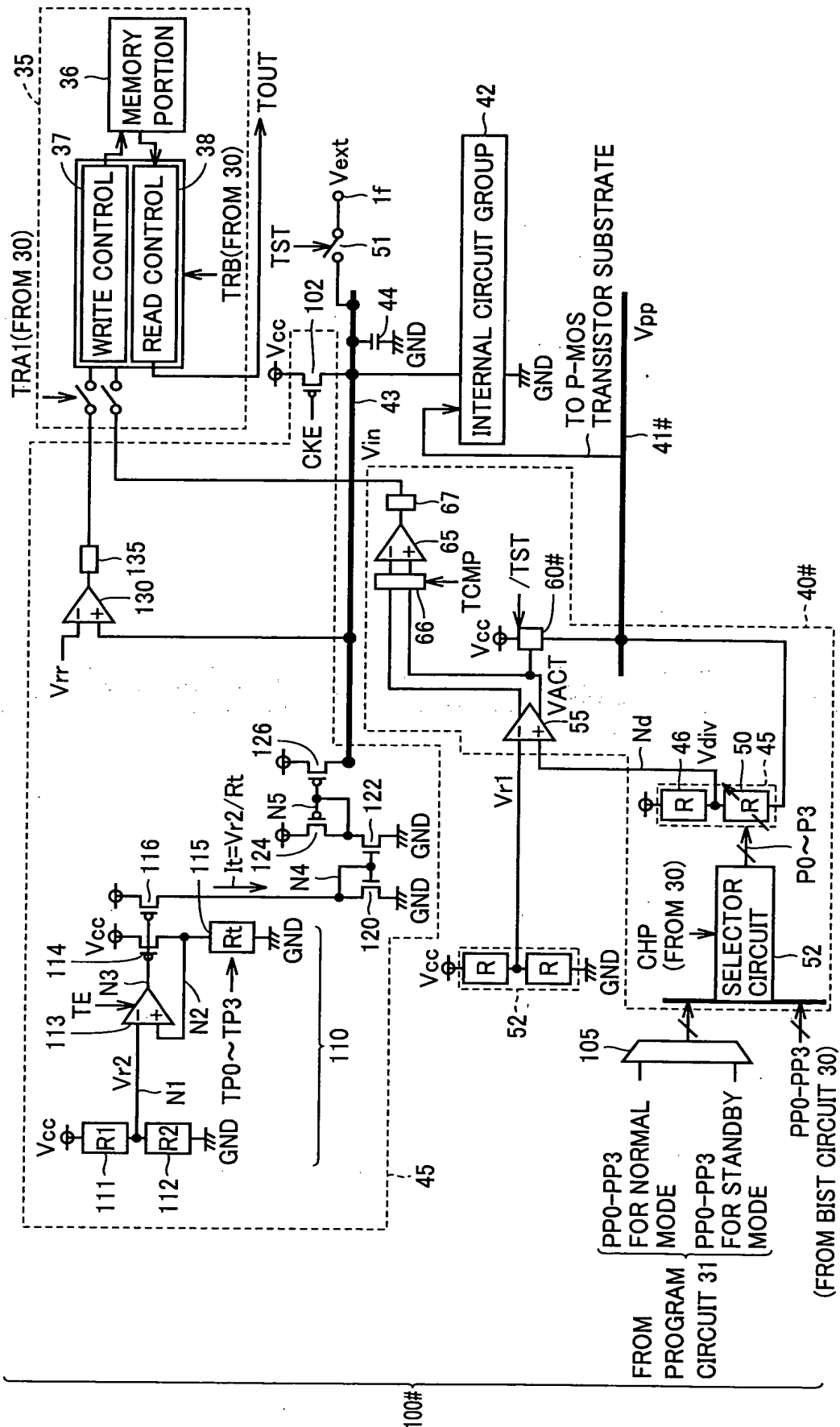


FIG.12

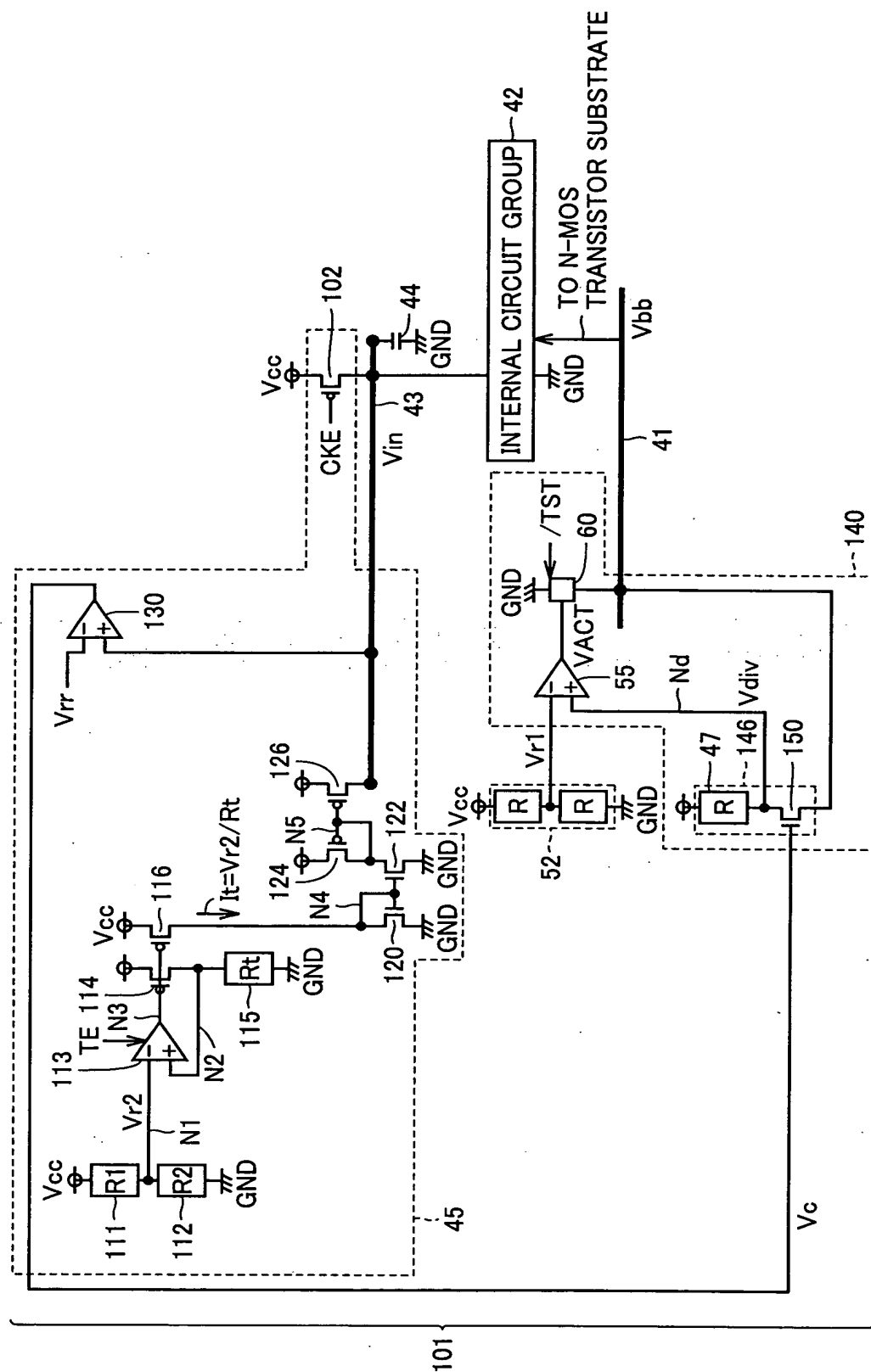


FIG. 13

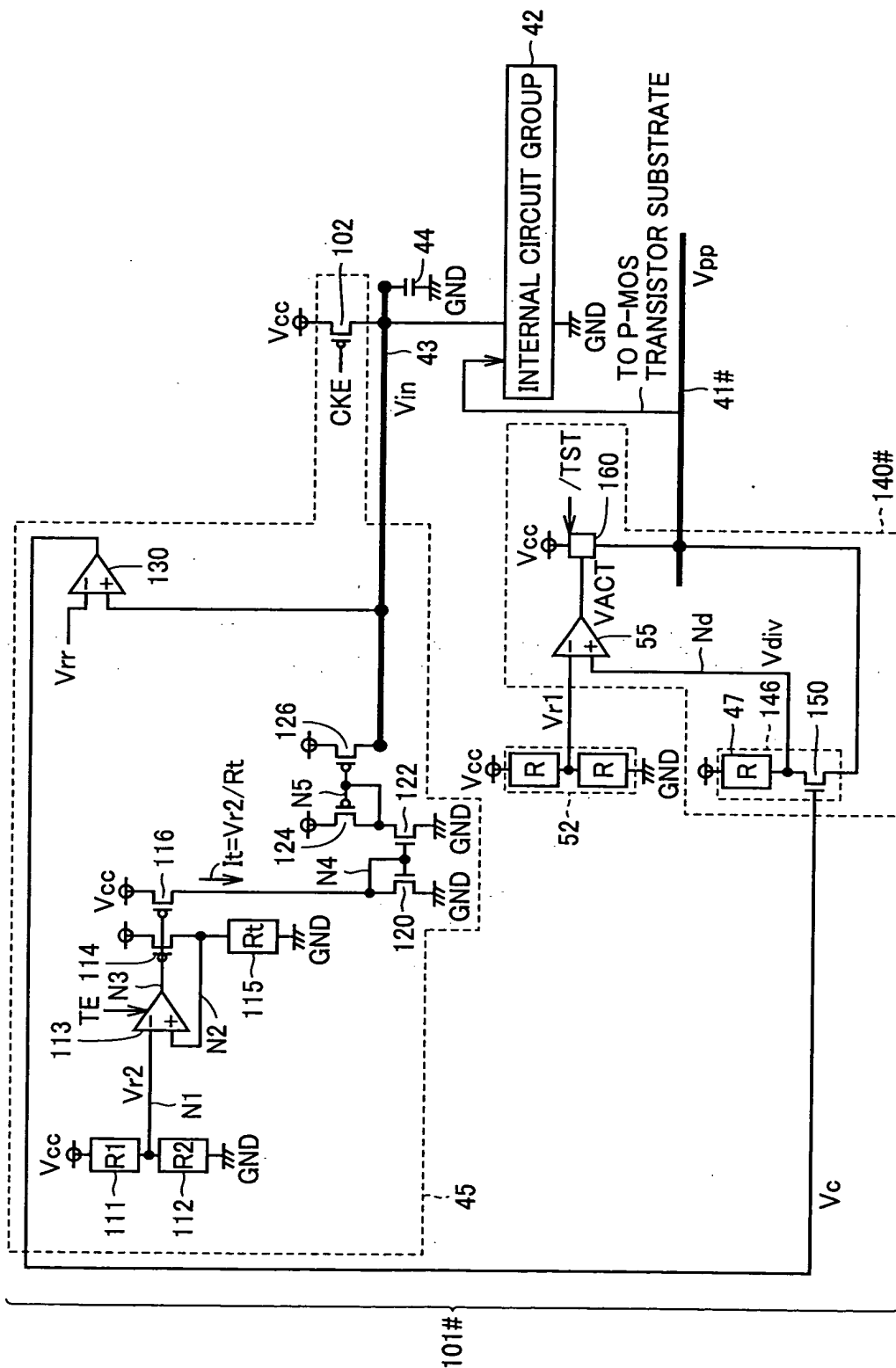


FIG.14

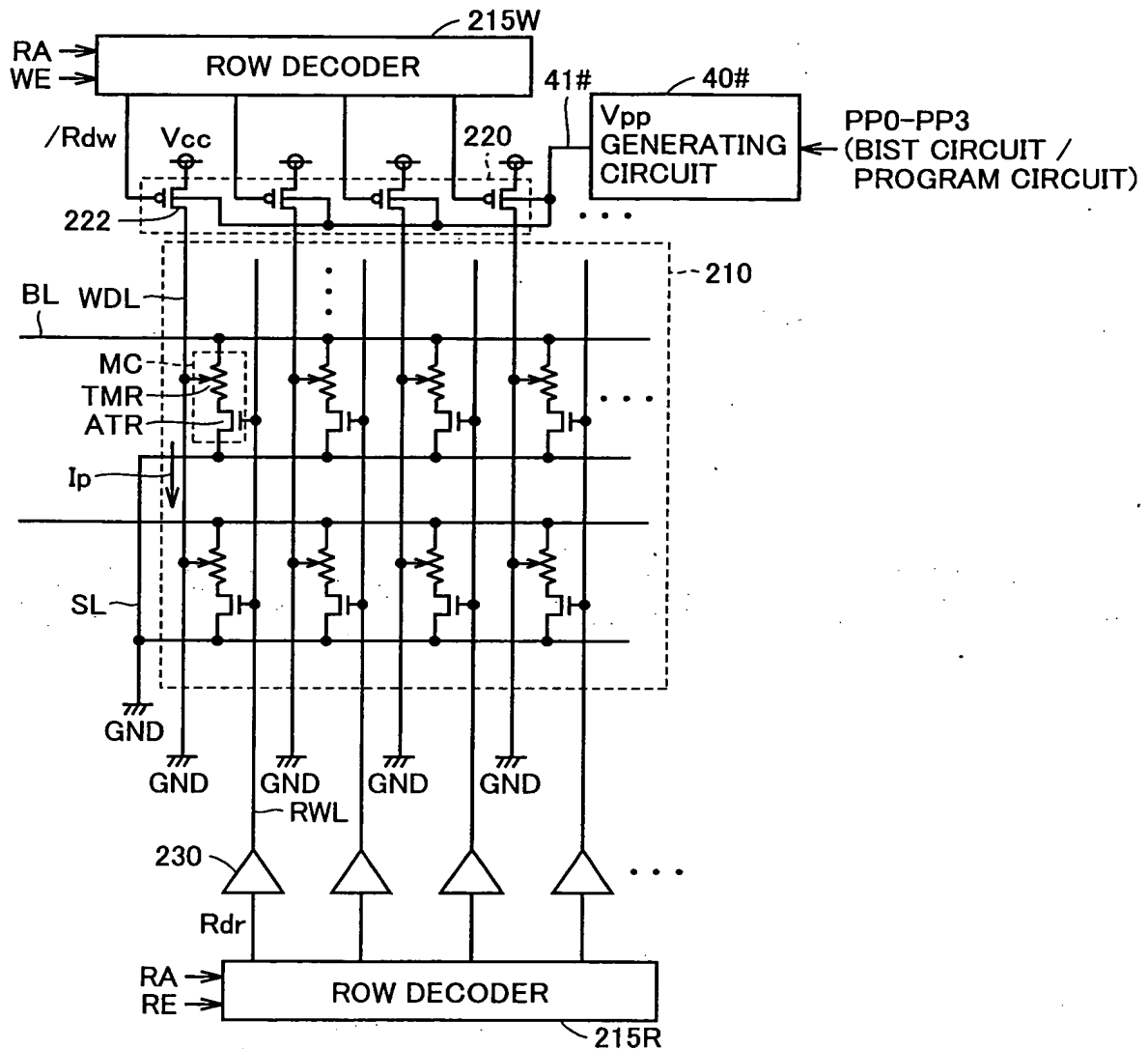


FIG.15

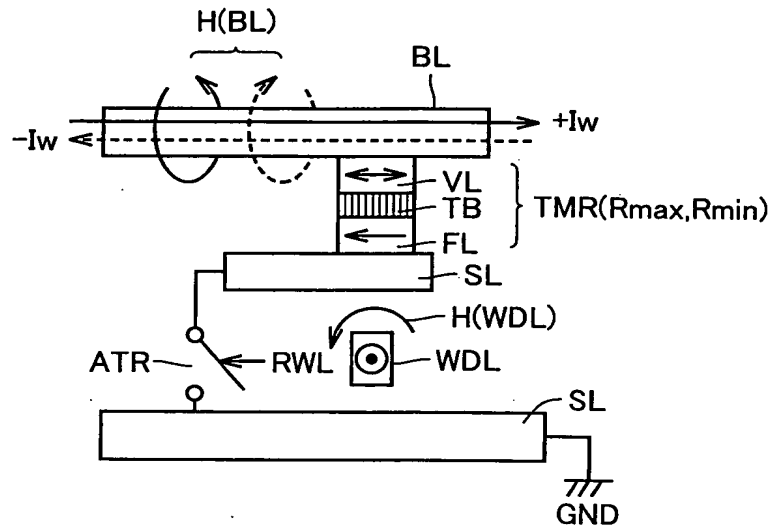


FIG.16

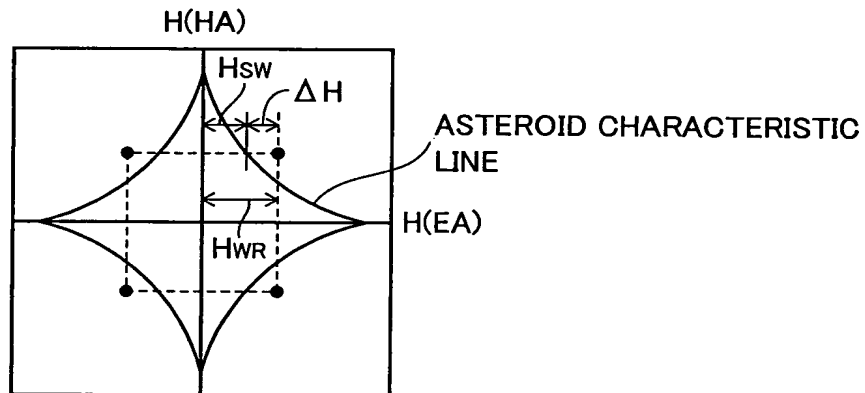


FIG.17

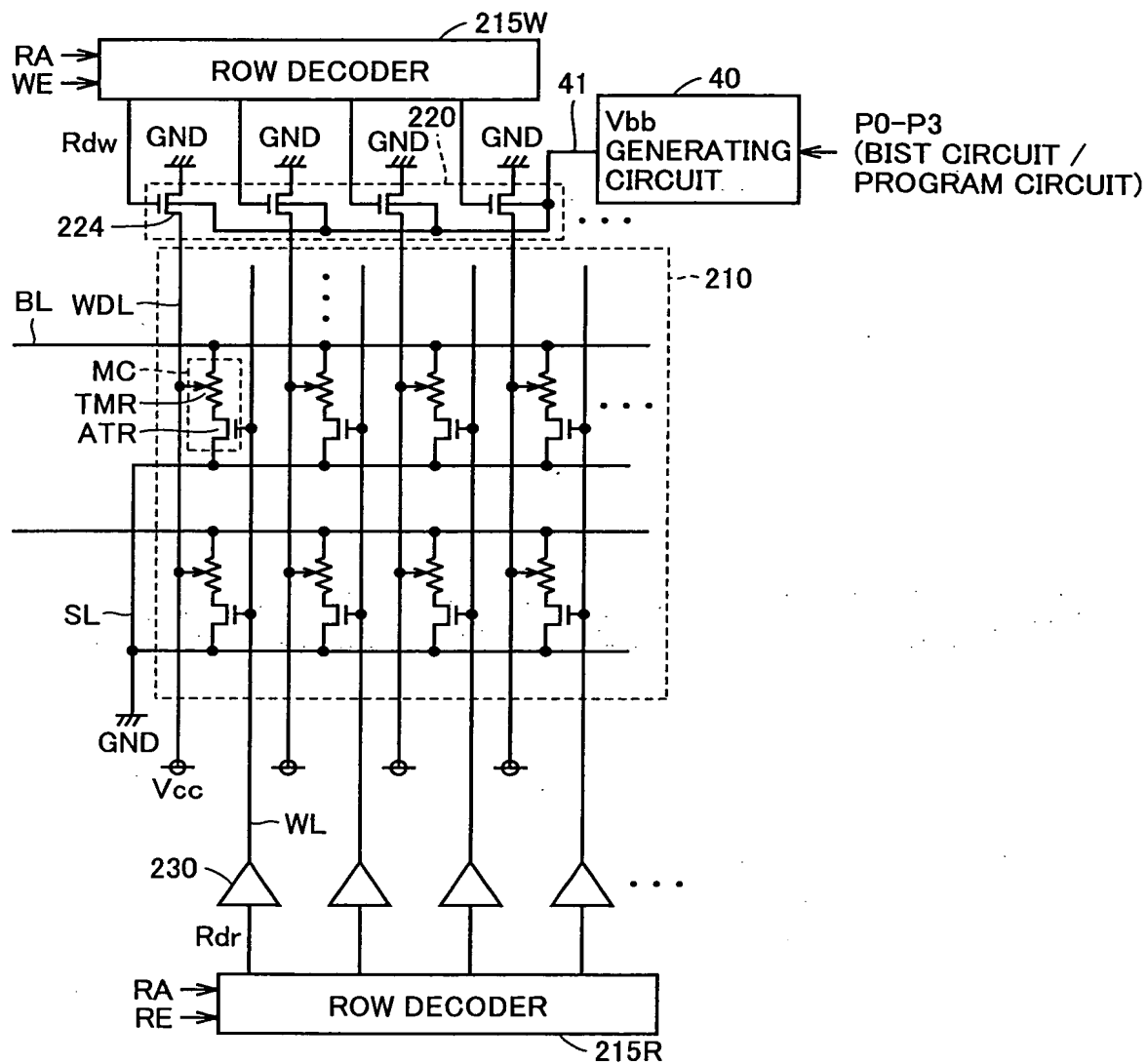


FIG.18

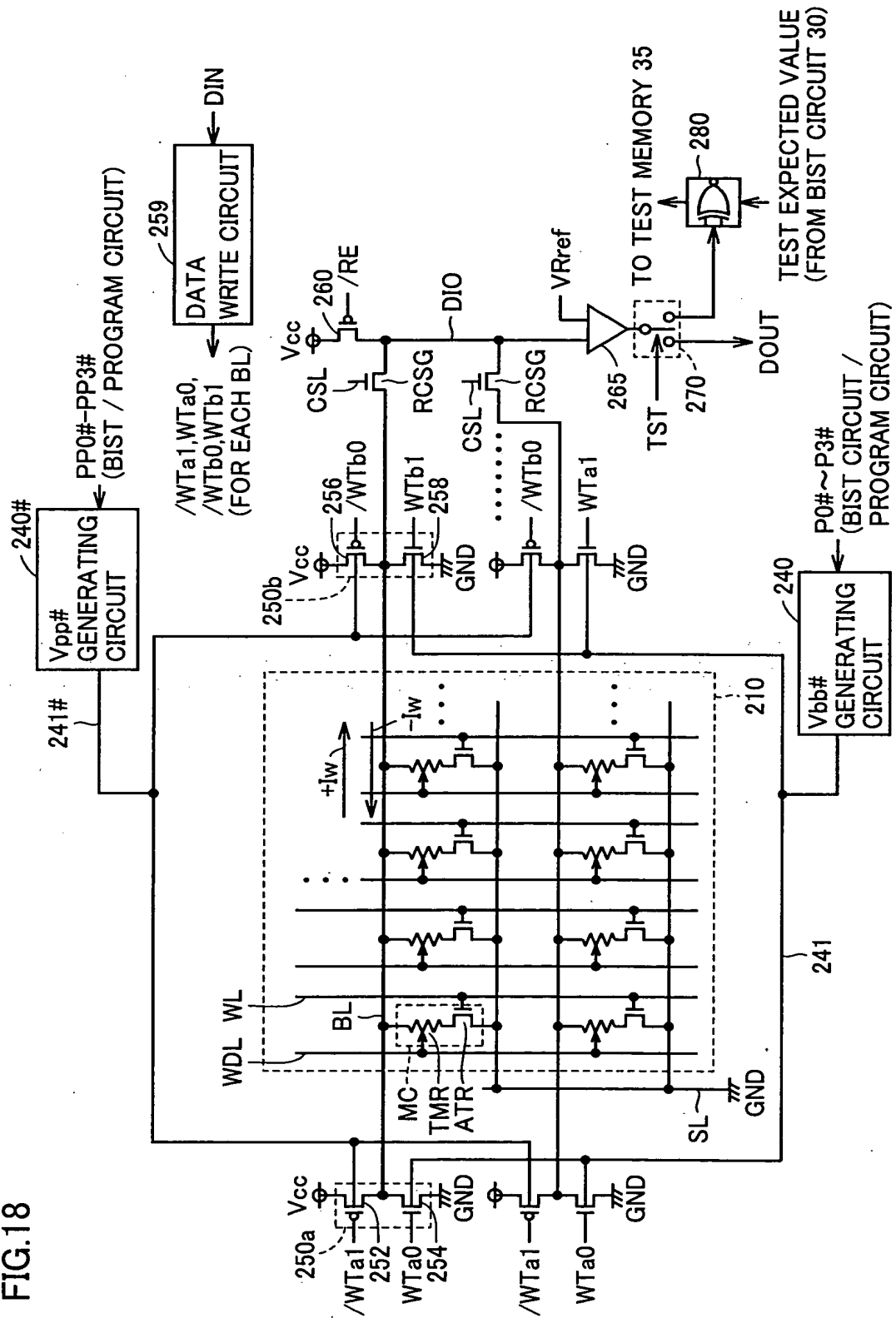


FIG.19

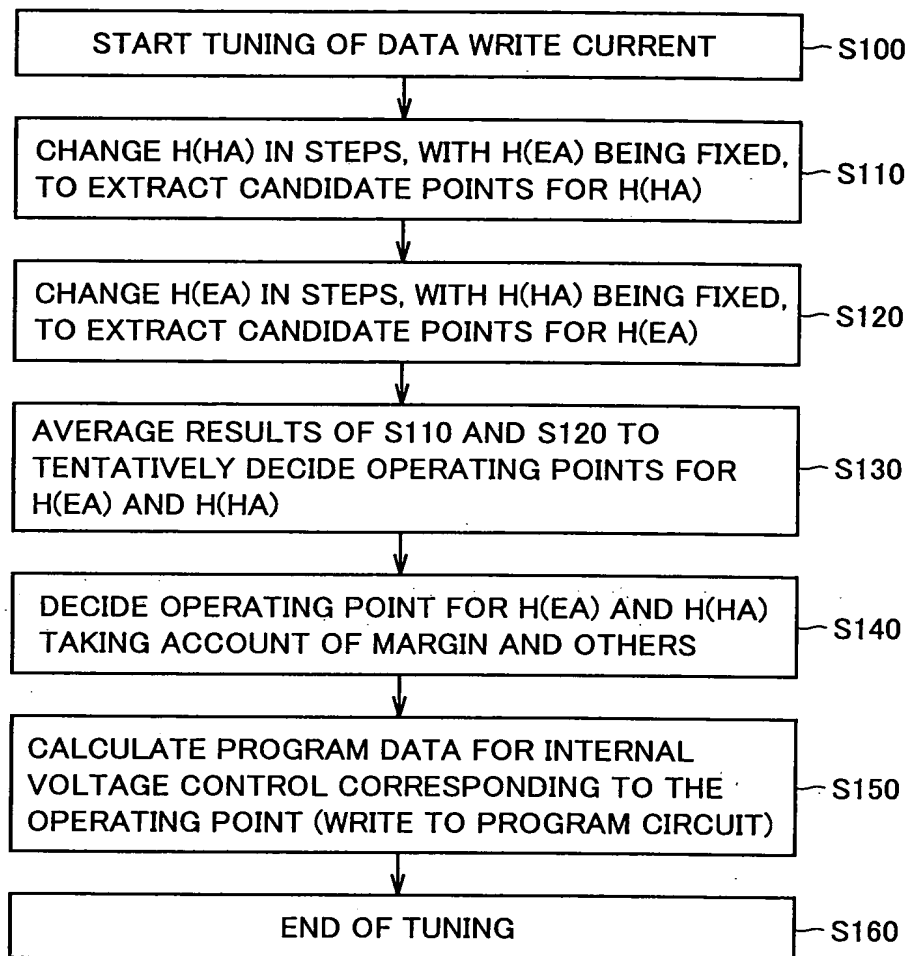


FIG.20

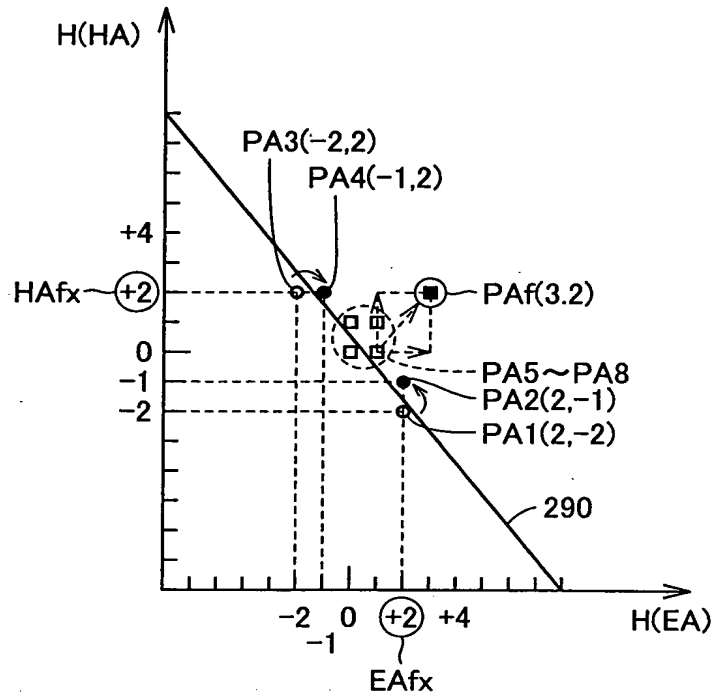


FIG.21

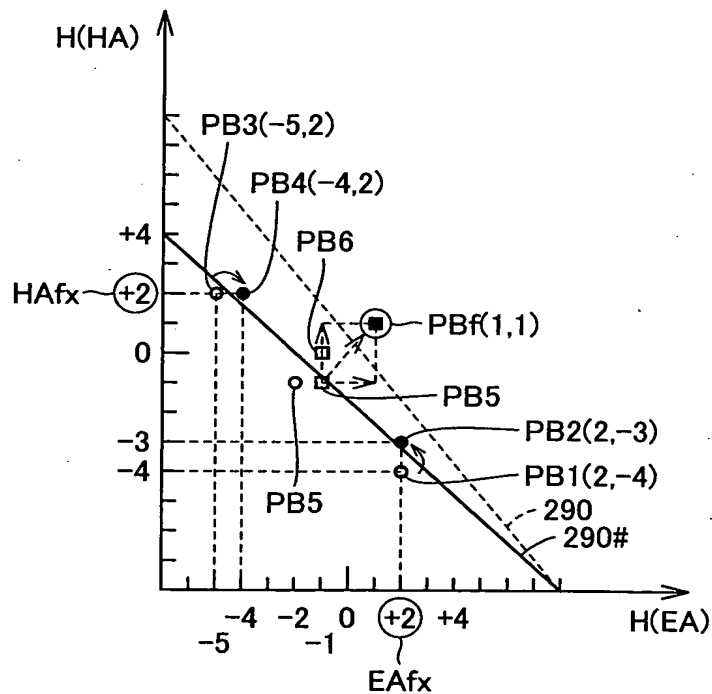


FIG.22

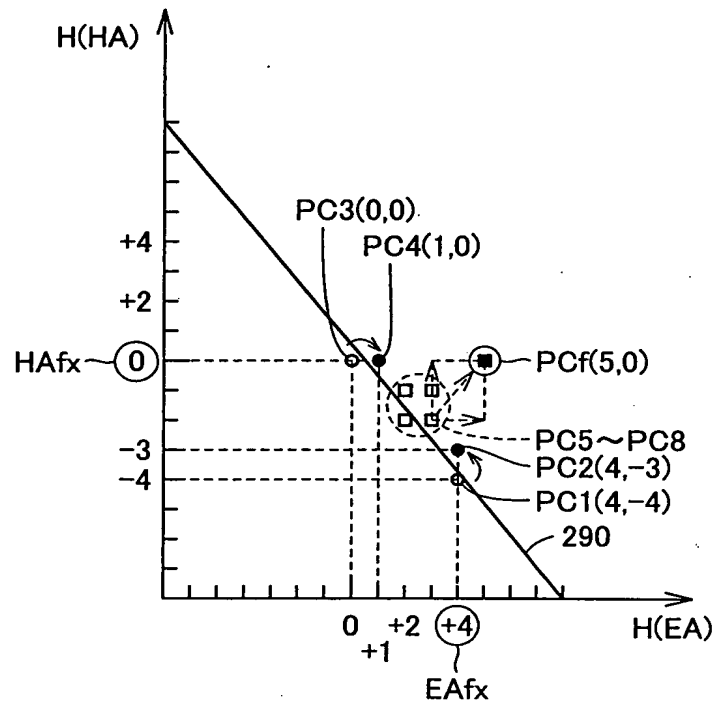


FIG.23

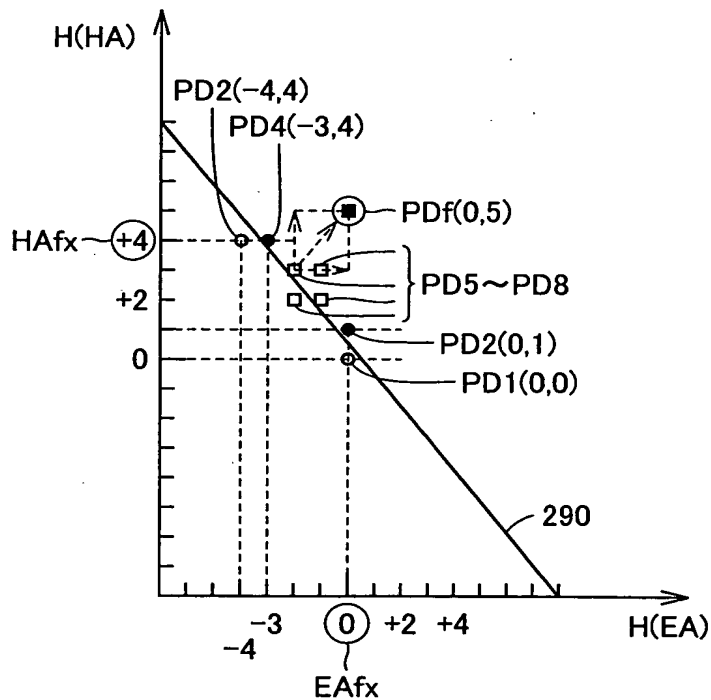
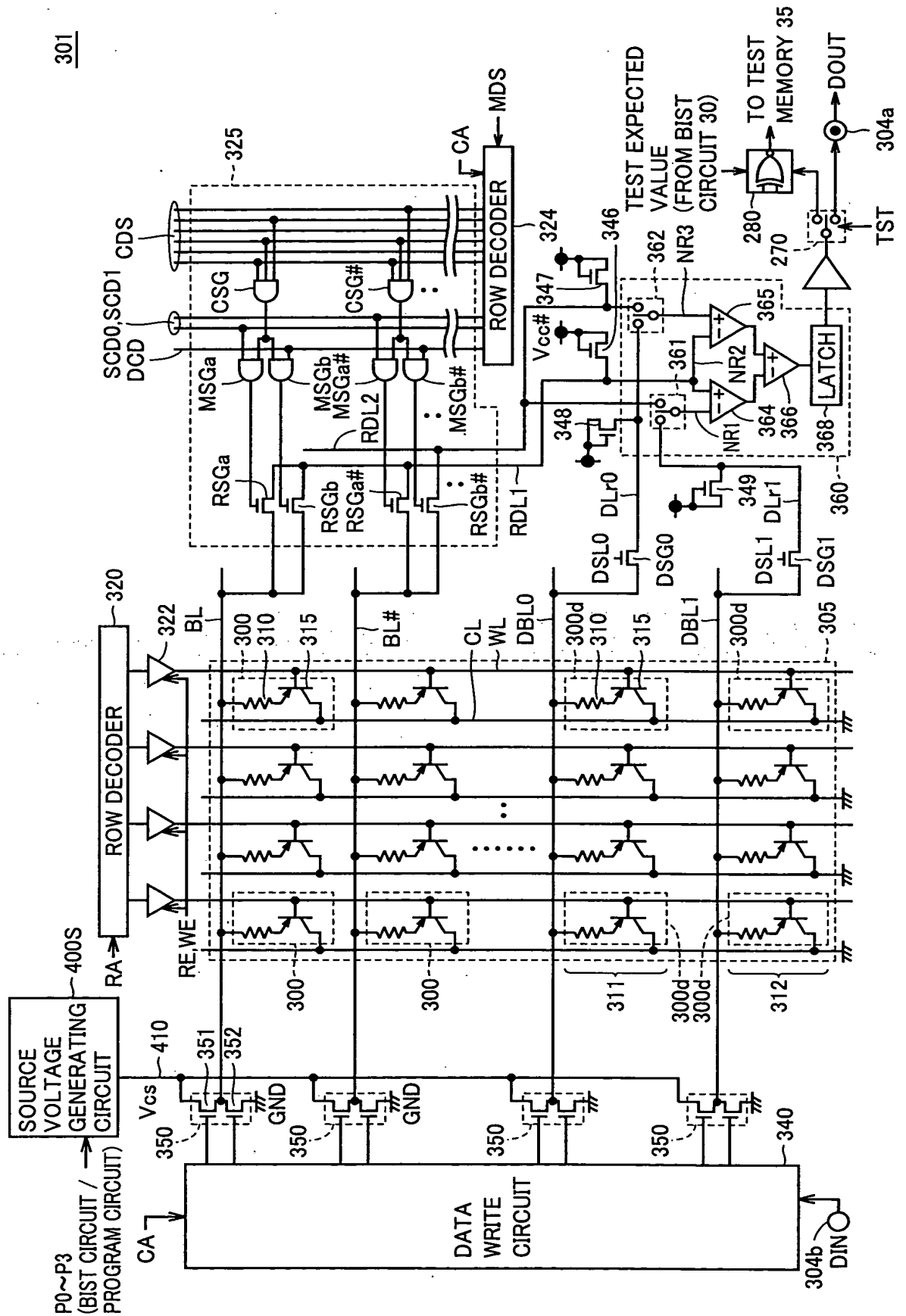


FIG.24



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FIG.25

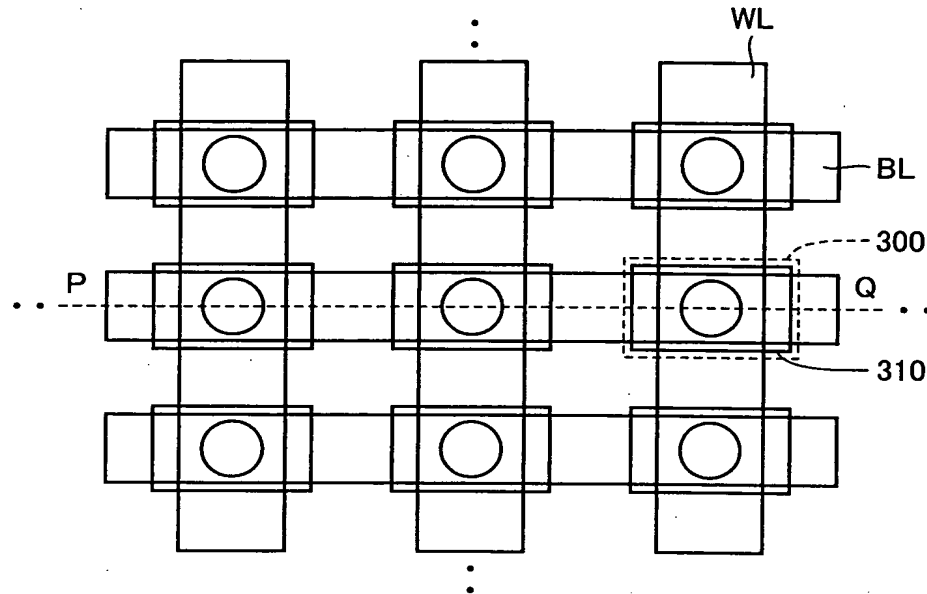


FIG.26

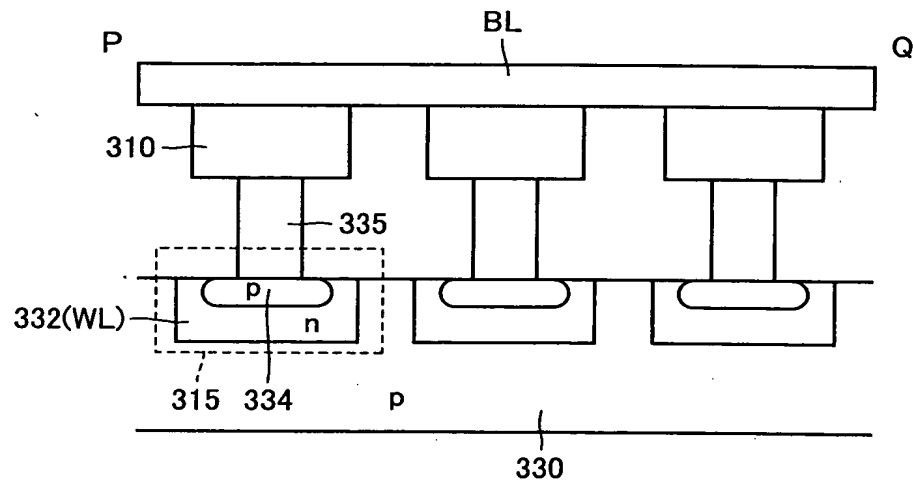


FIG.28A

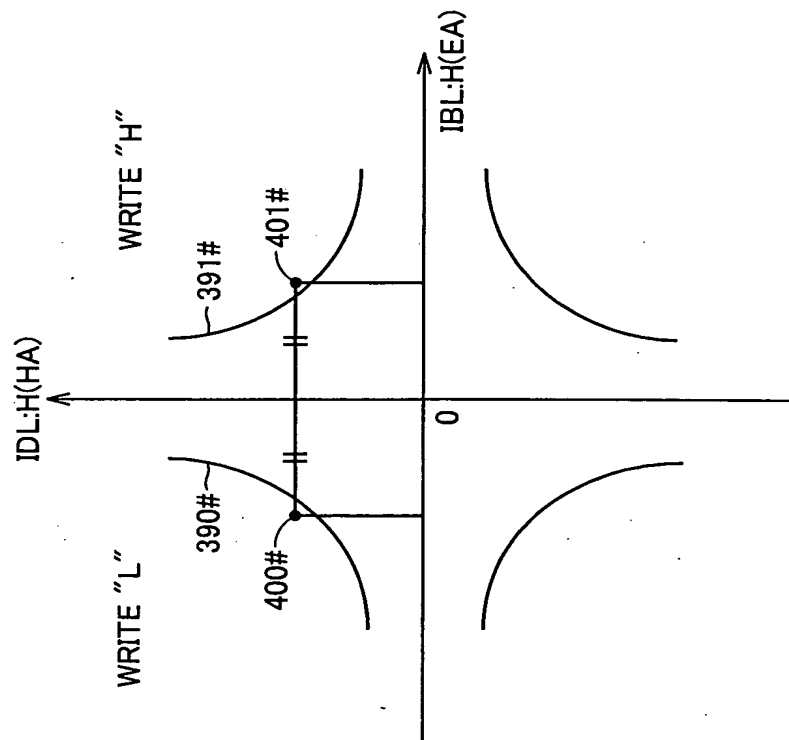


FIG.28B

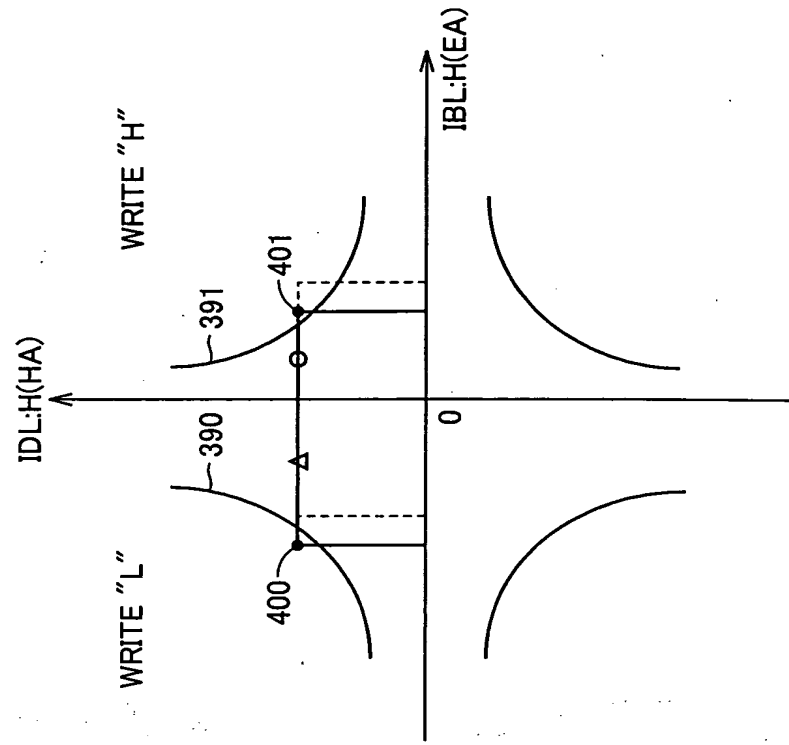


FIG.29A

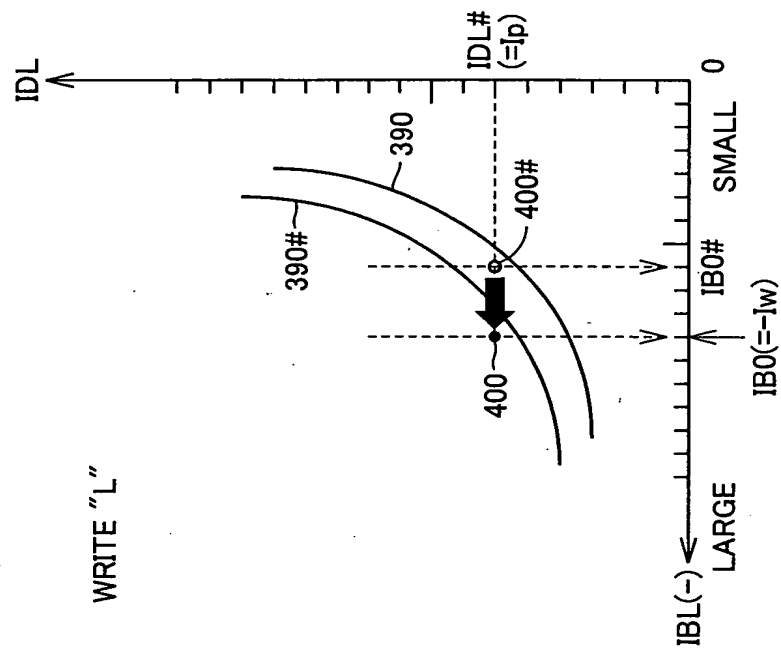


FIG.29B

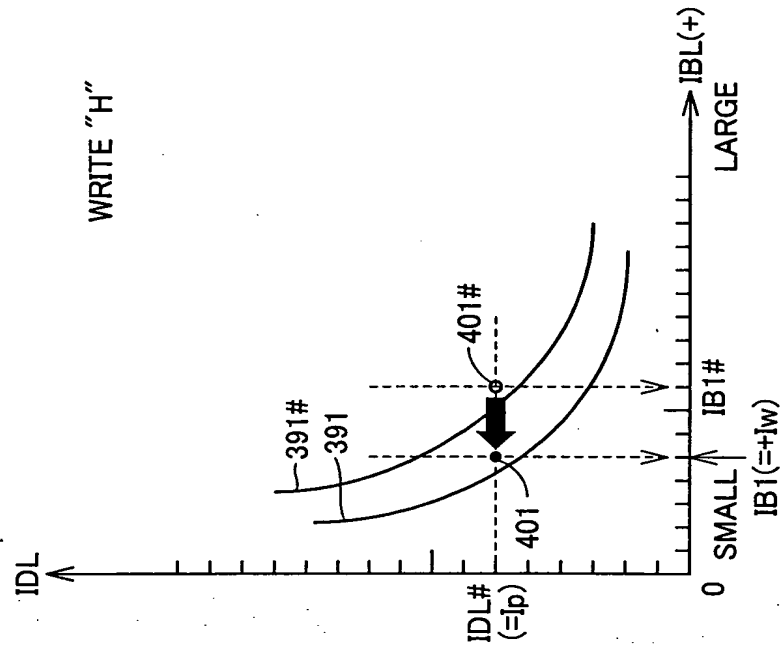


FIG.30

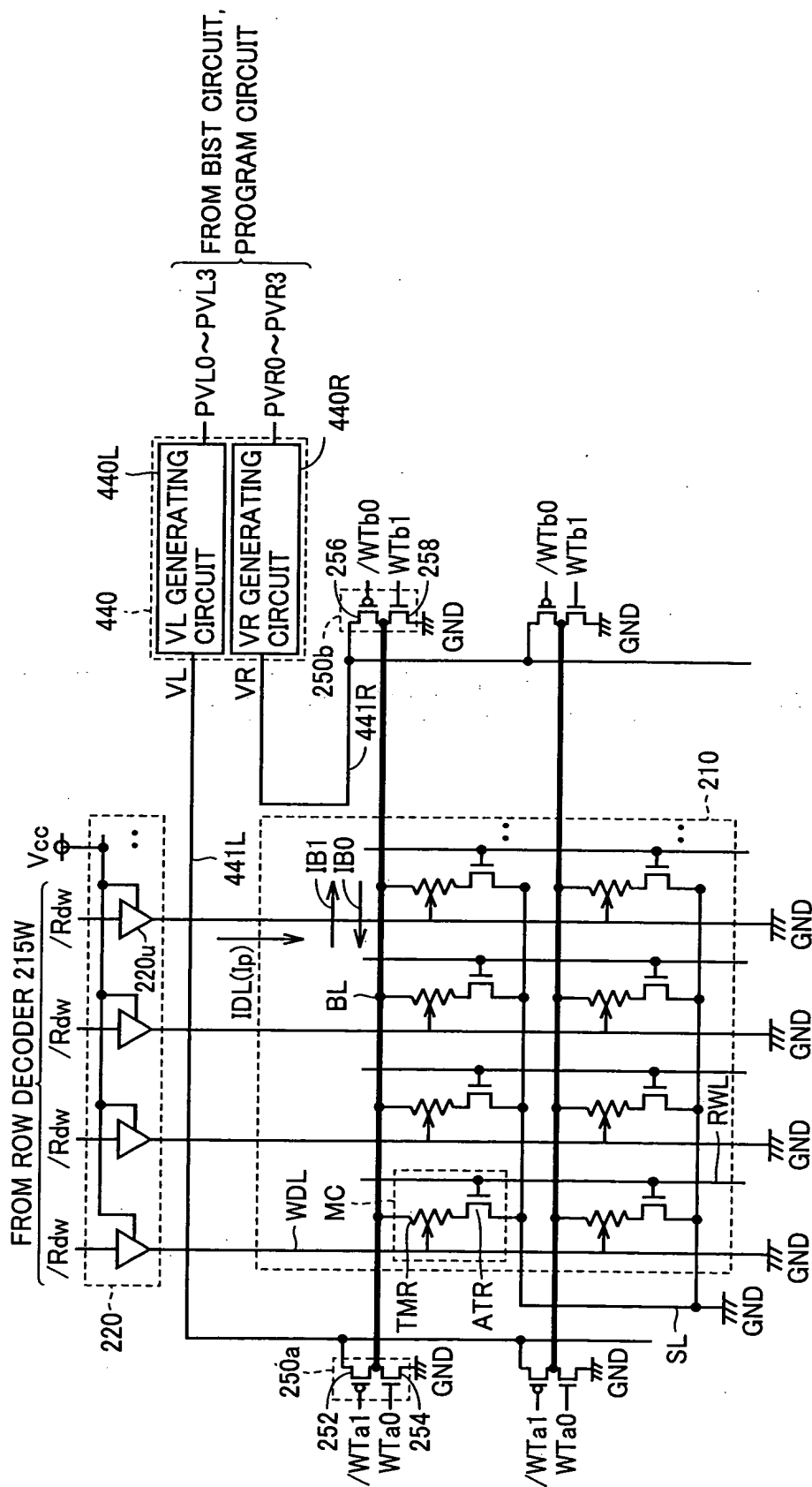


FIG.31A

WRITE "L"

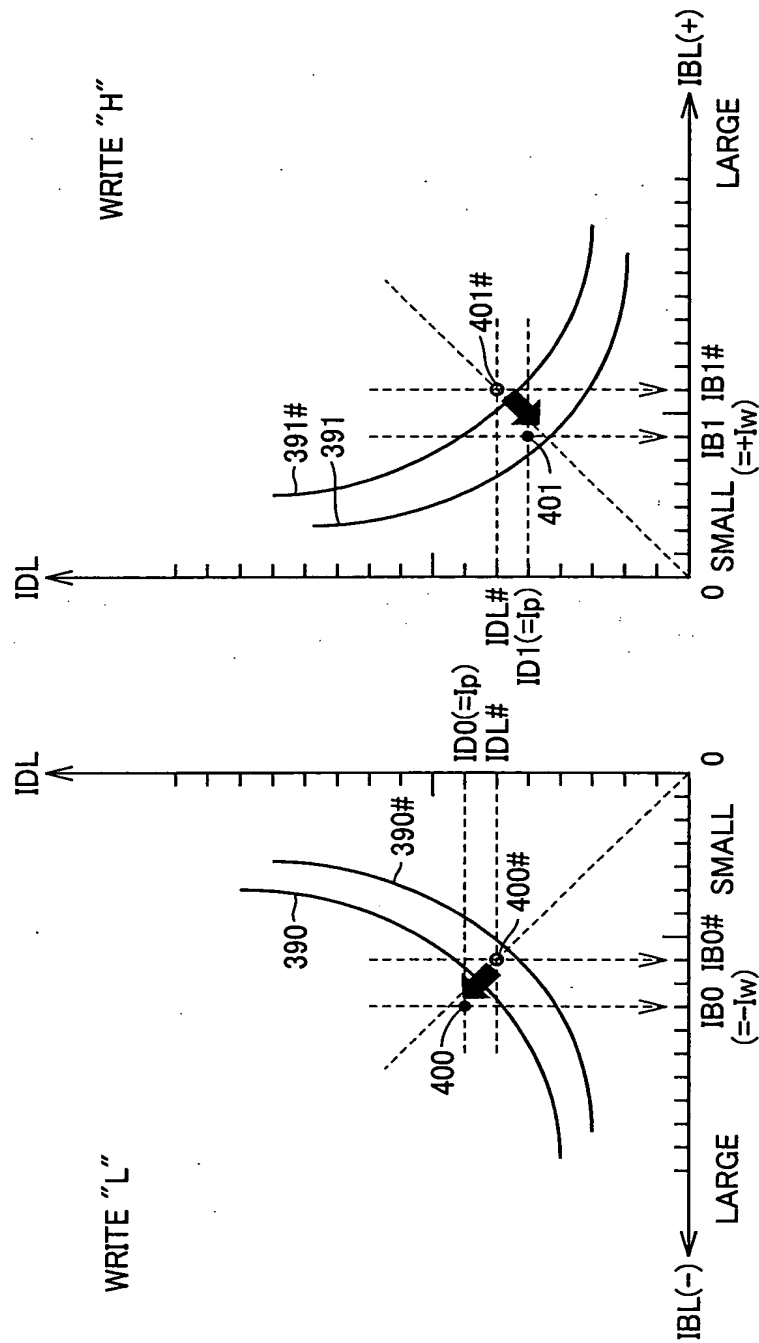


FIG. 31B

WRITE "H"

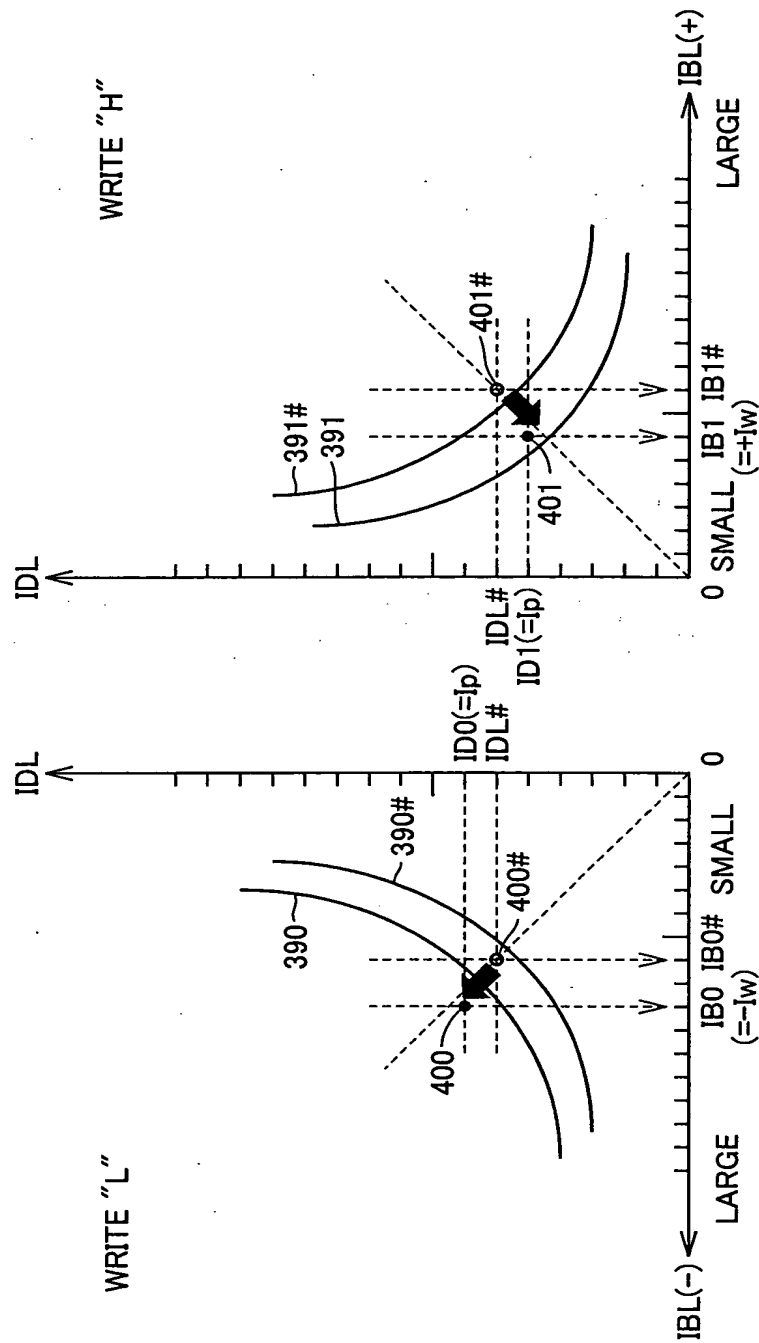


FIG. 32

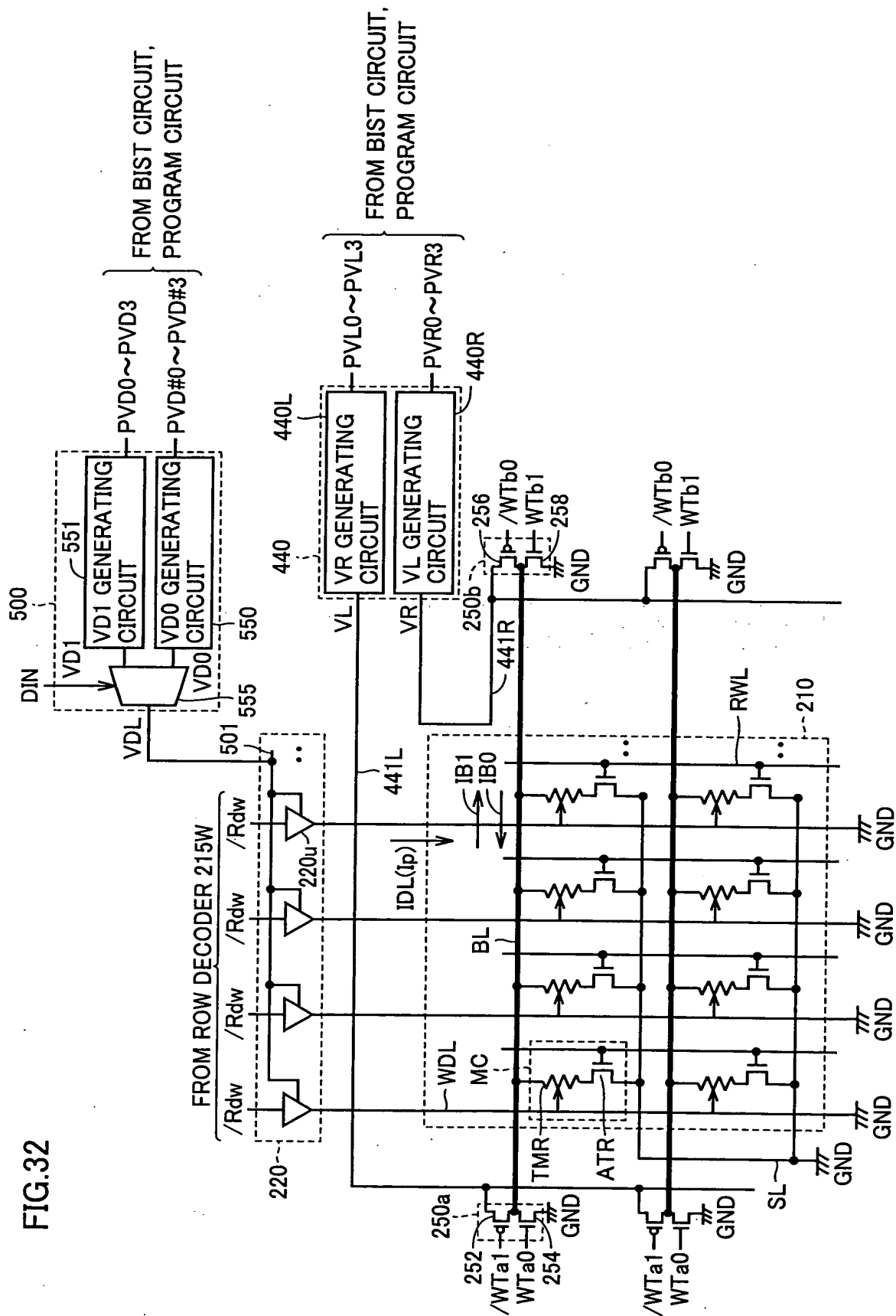


FIG. 33

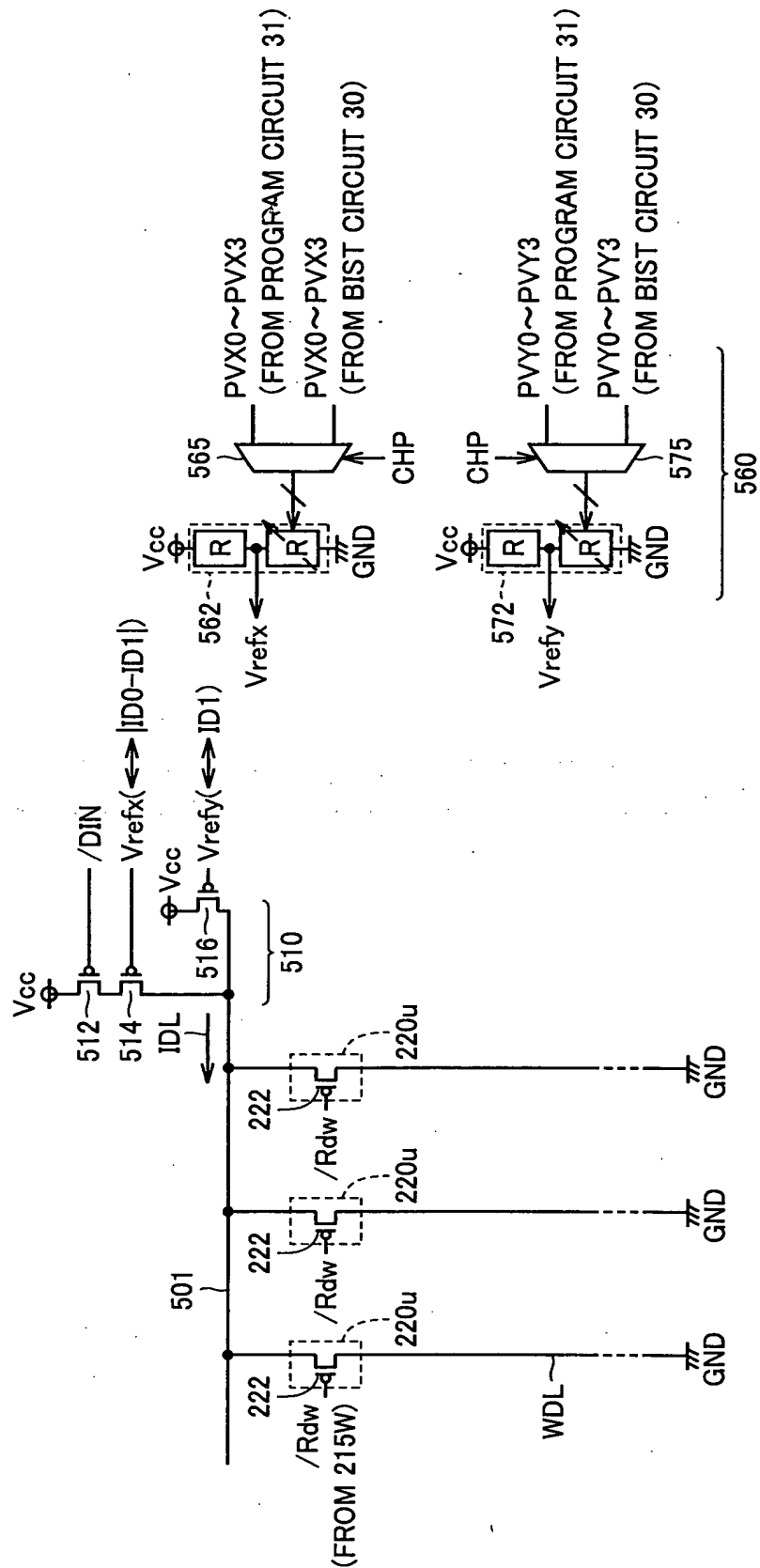


FIG.34

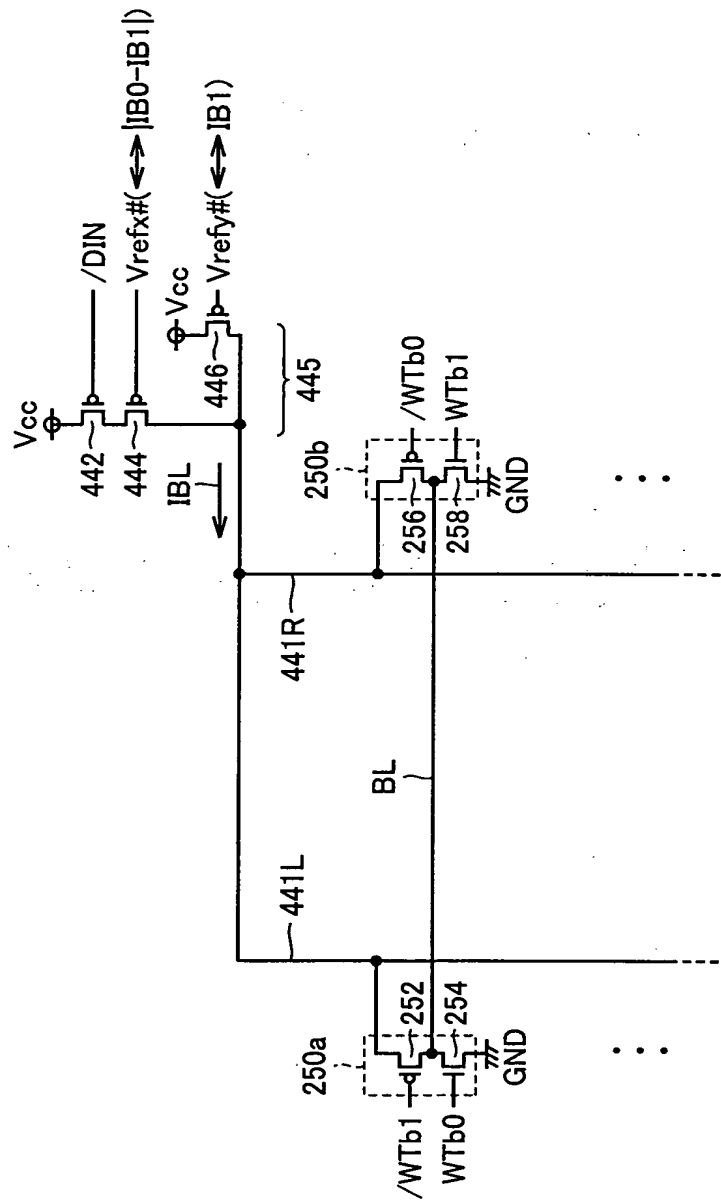


FIG.35

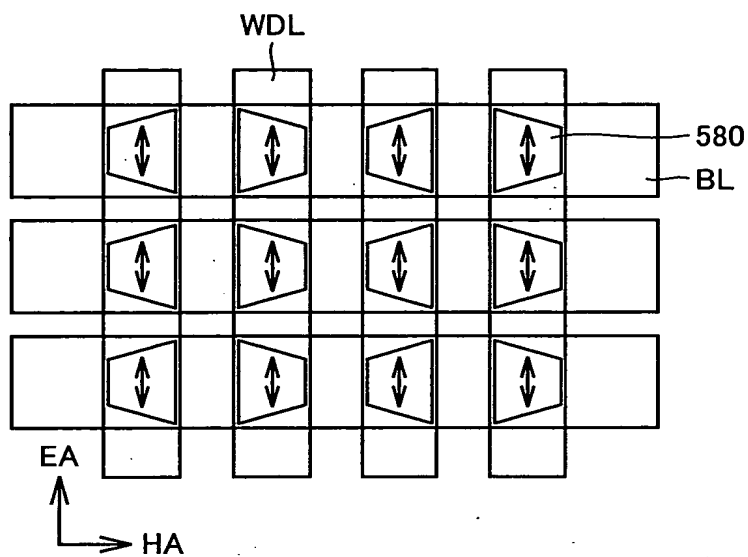


FIG.36

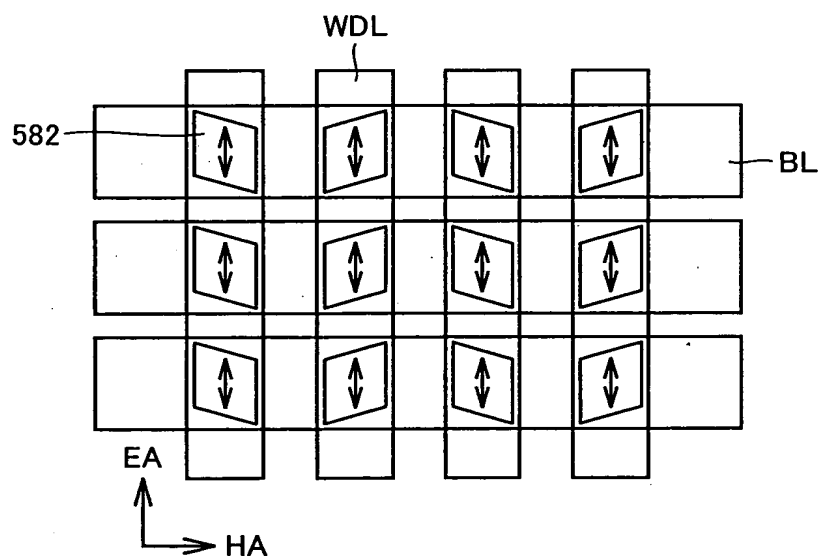


FIG.37

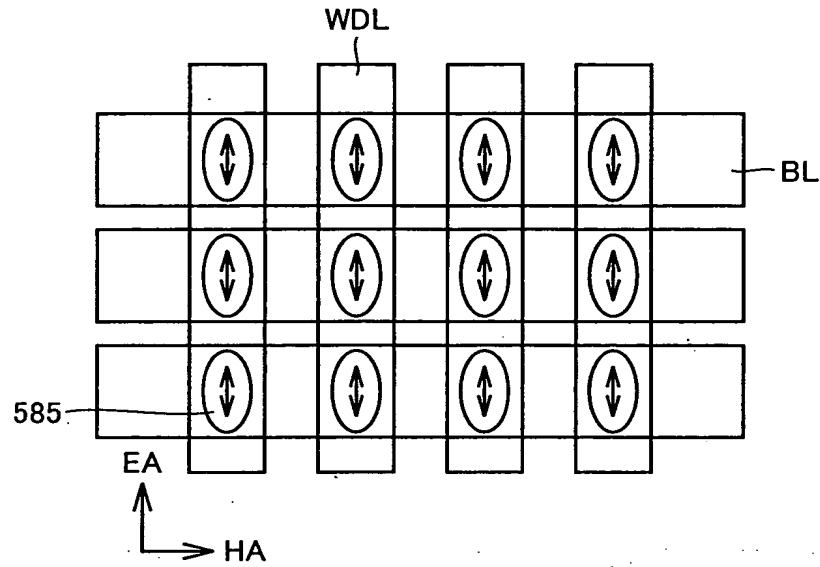


FIG.38A

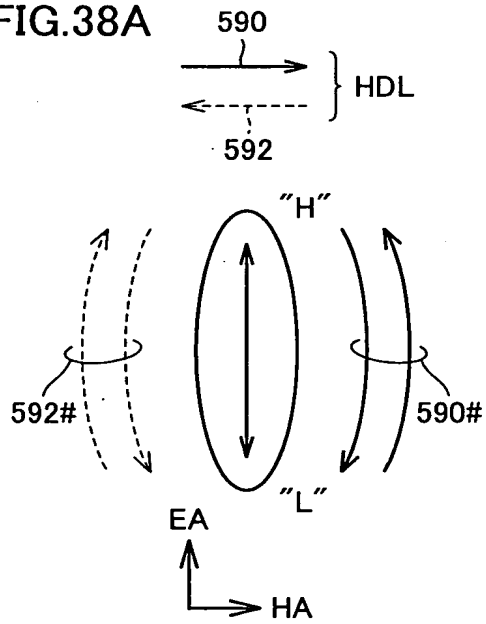


FIG.38B

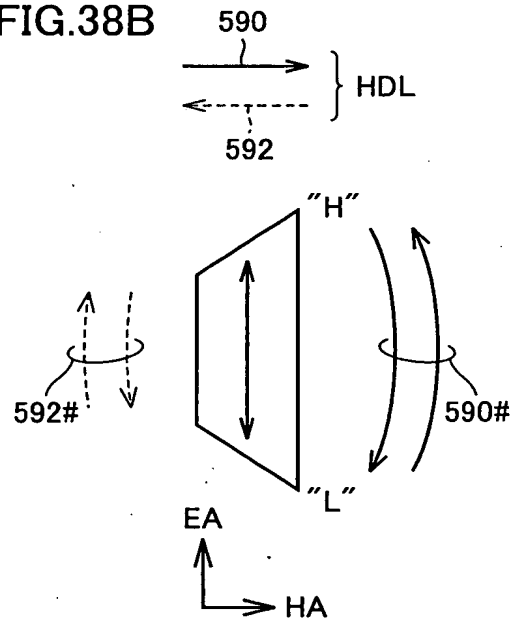


FIG.39A

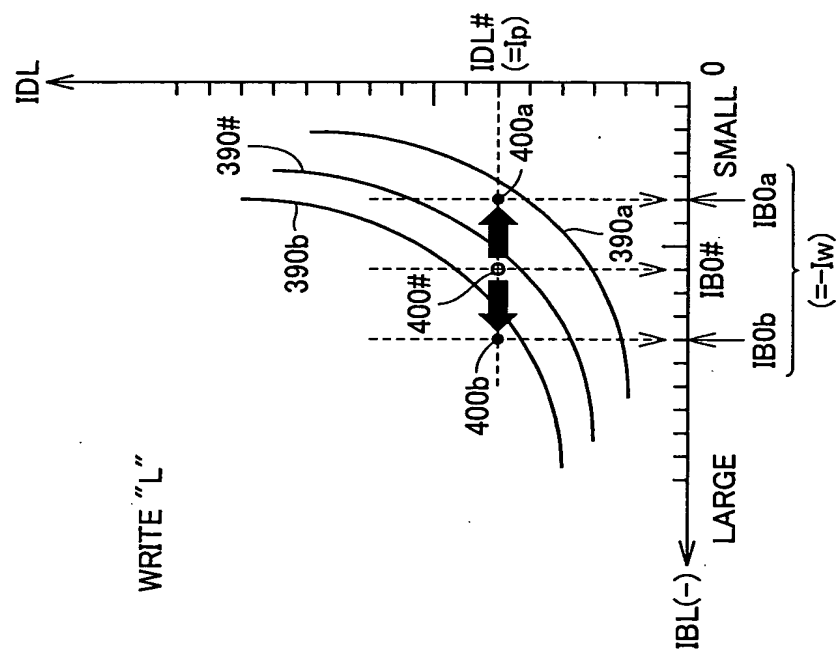


FIG.39B

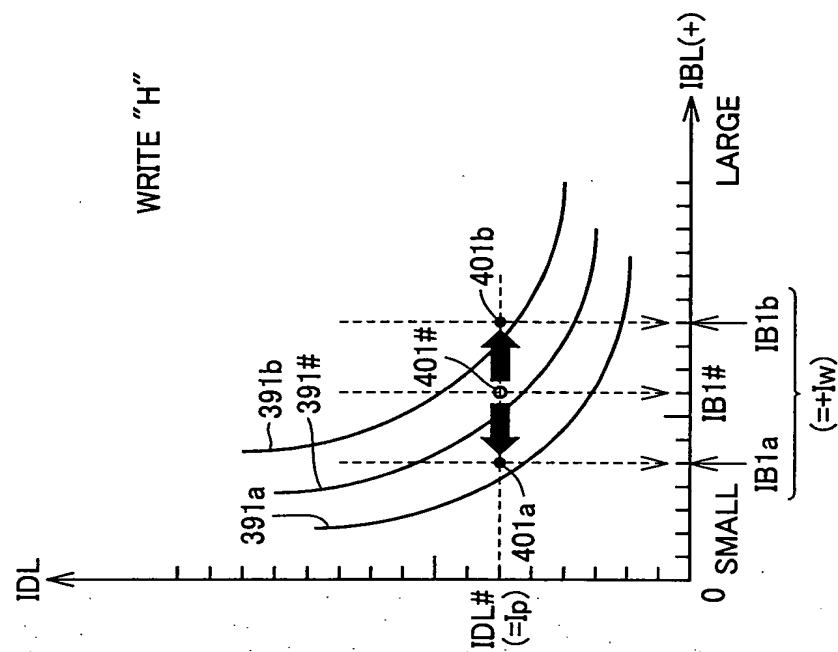


FIG.41

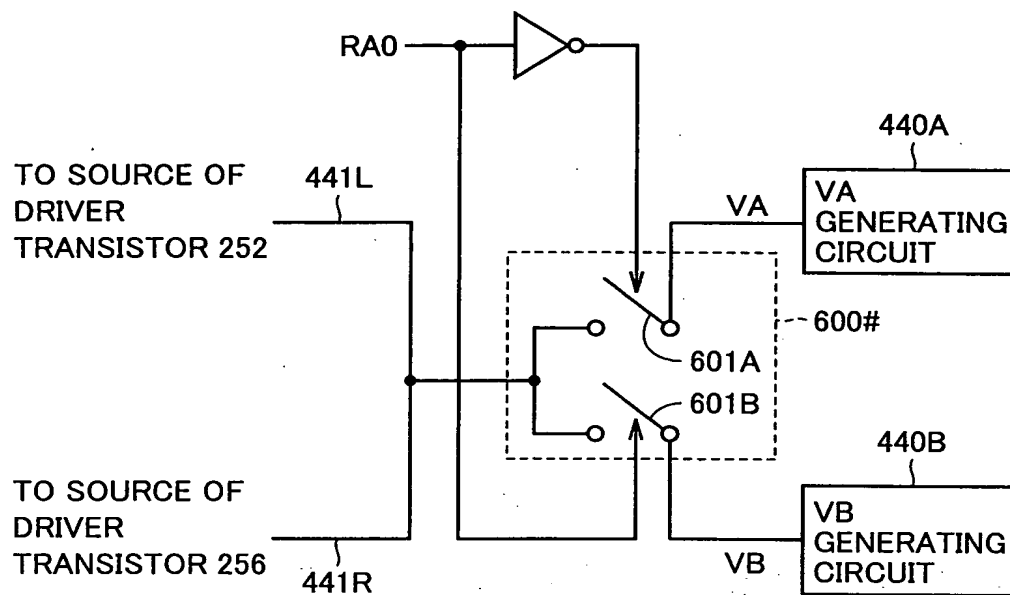


FIG.42

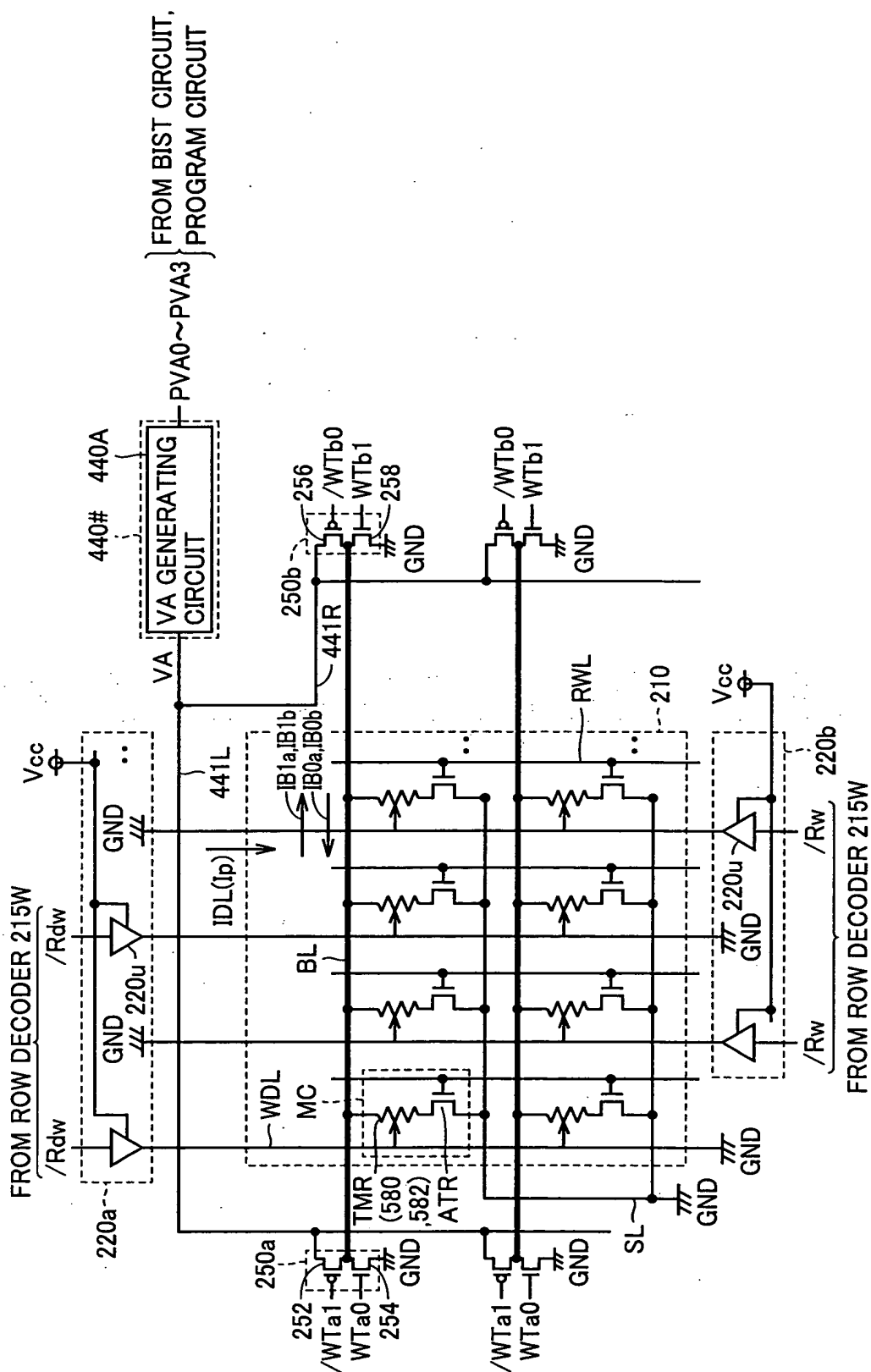


FIG.43A

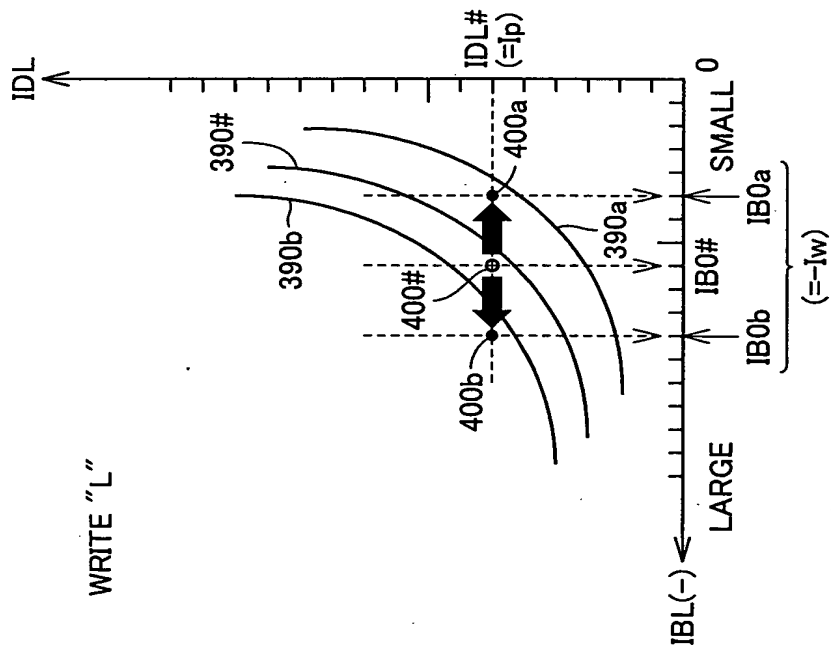


FIG.43B

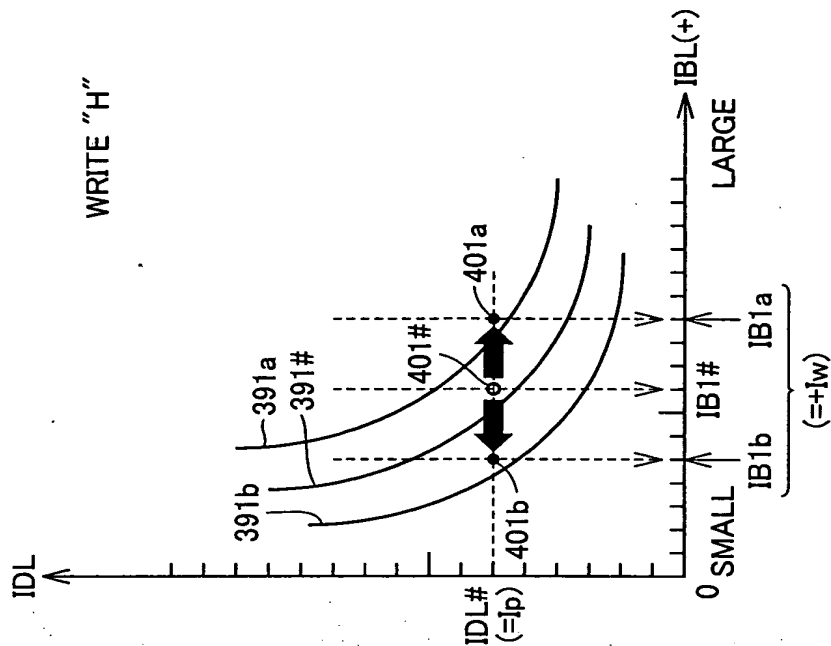


FIG.45

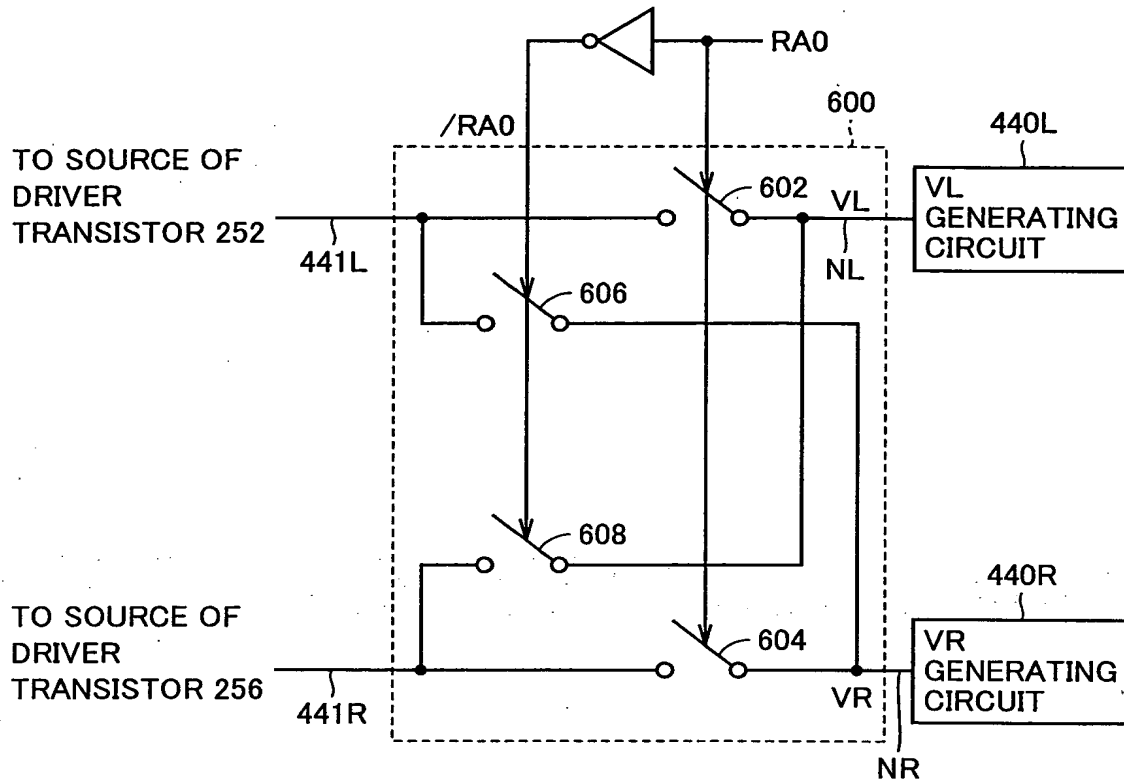


FIG.46

